

FIG. 1
PRIOR ART

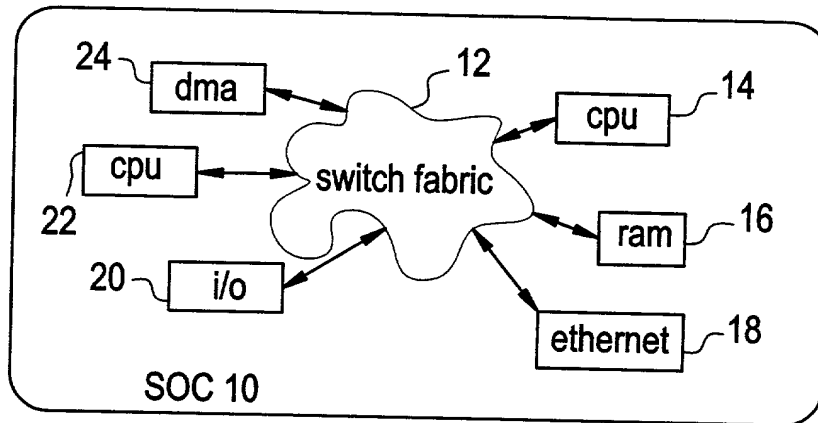


FIG. 2

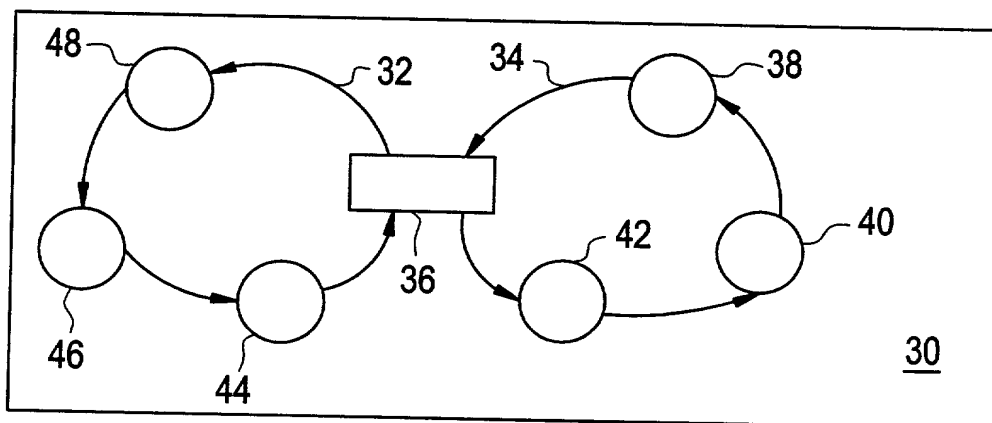


FIG. 3

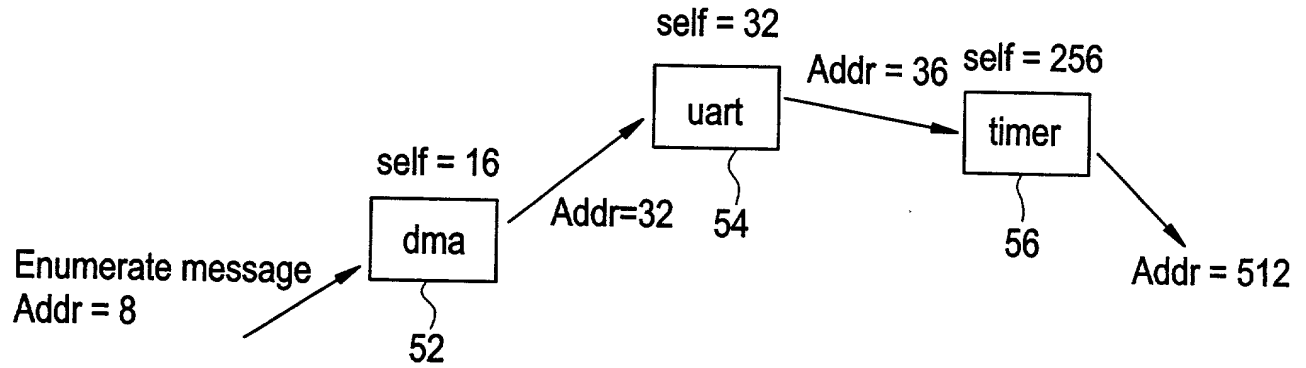


FIG. 4

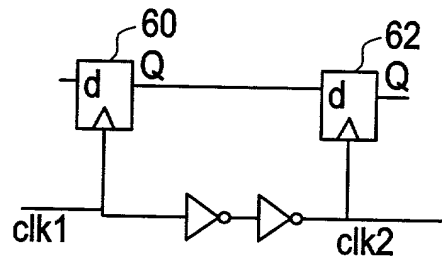


FIG. 5

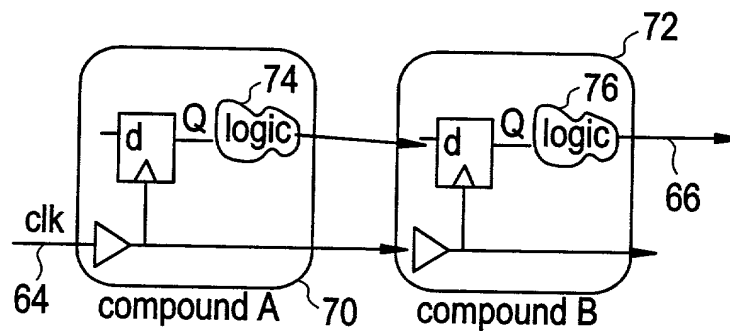


FIG. 6

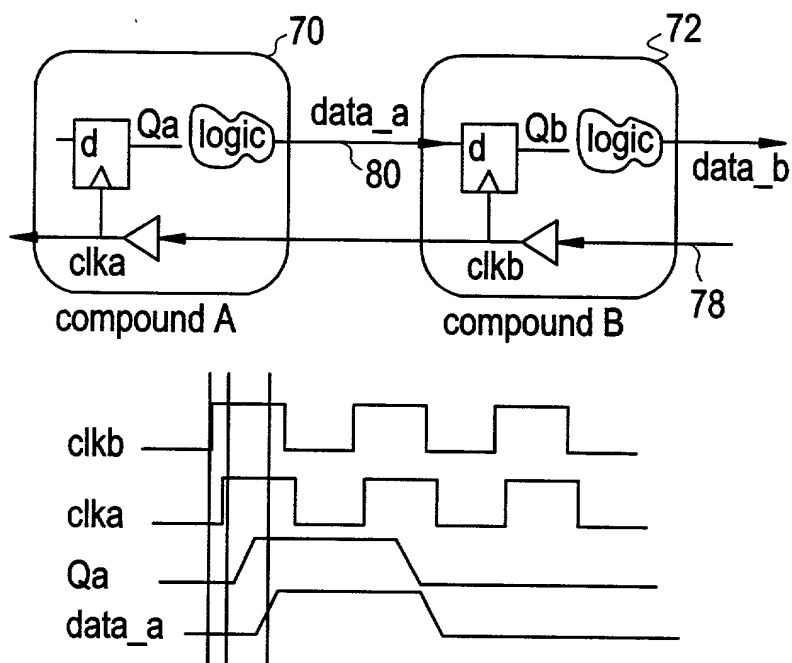


FIG. 7

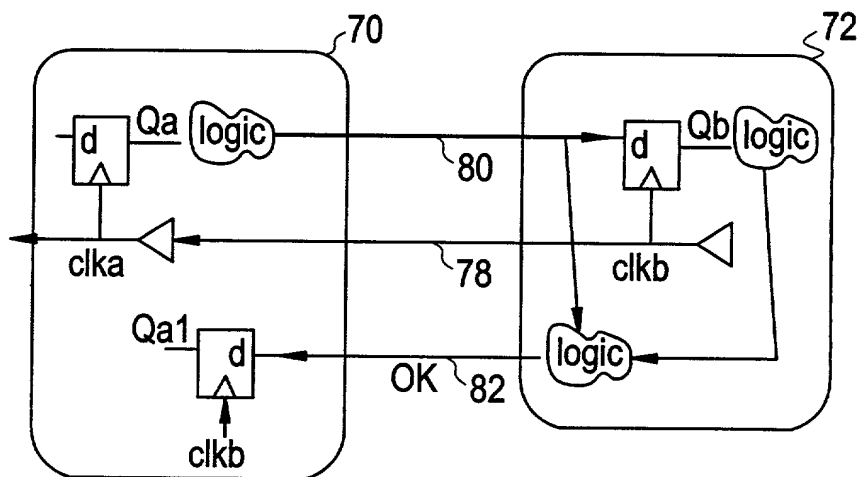


FIG. 10

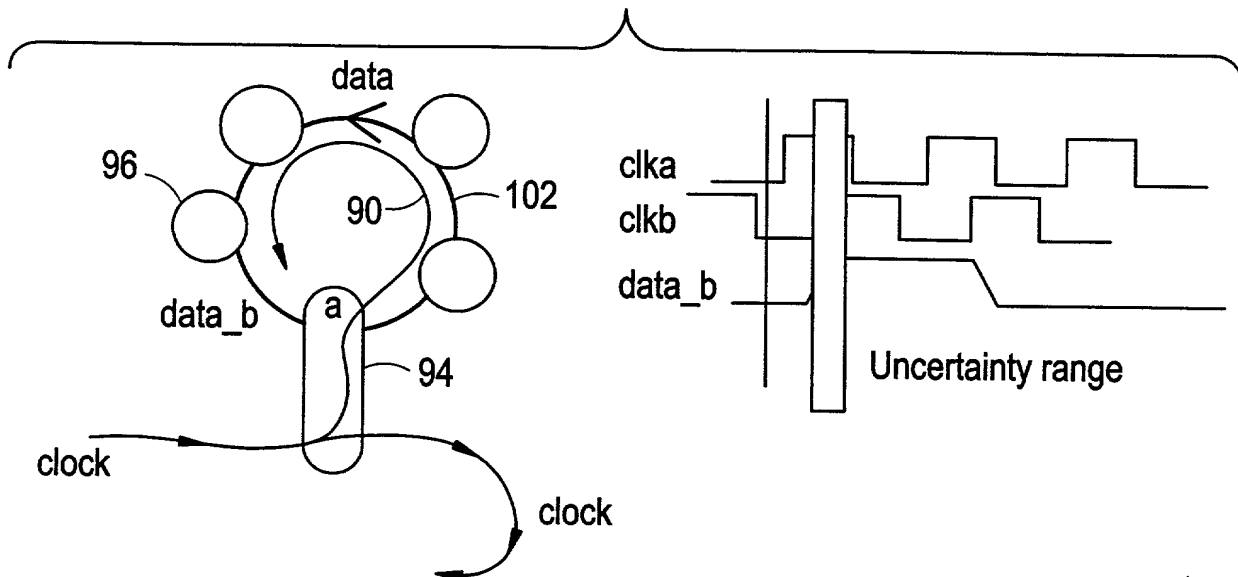


FIG. 11

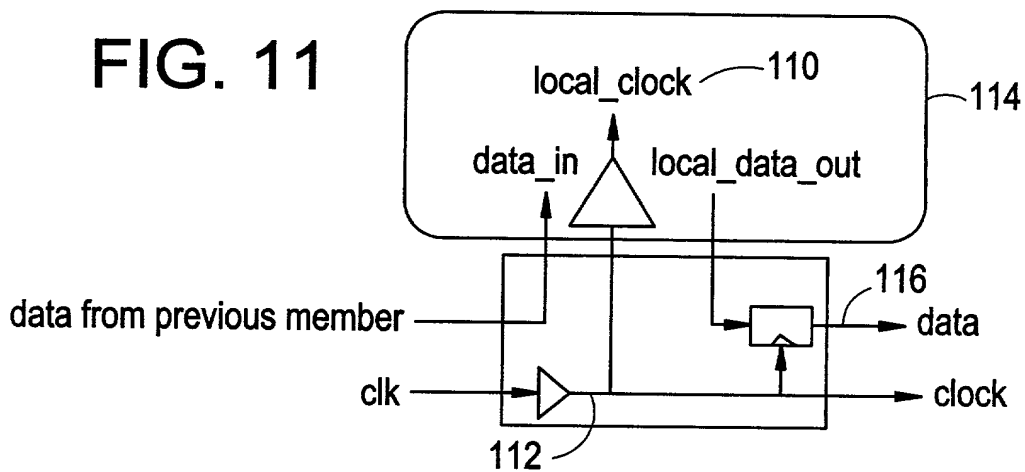


FIG. 12

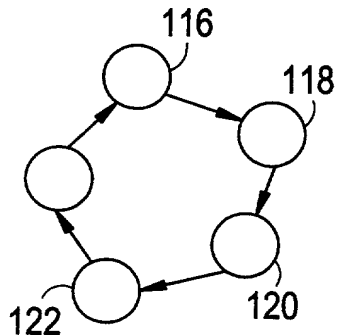


FIG. 13

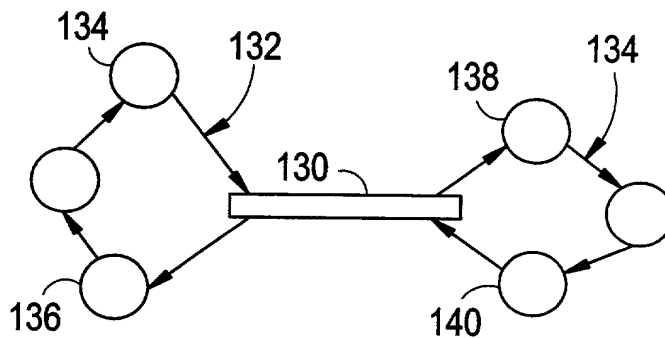


FIG. 14

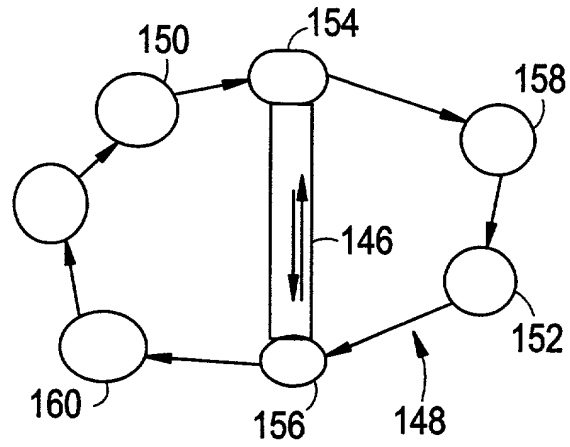


FIG. 15

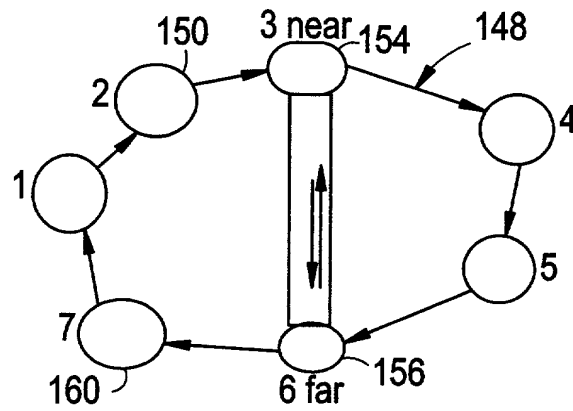


FIG. 16

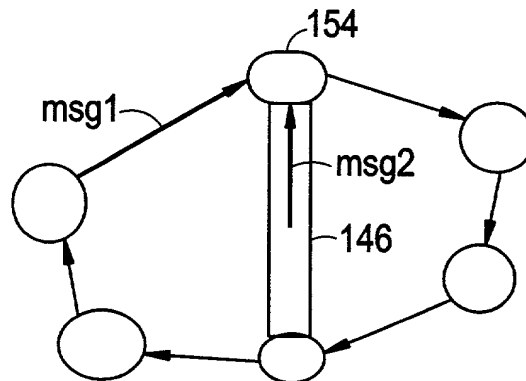


FIG. 17

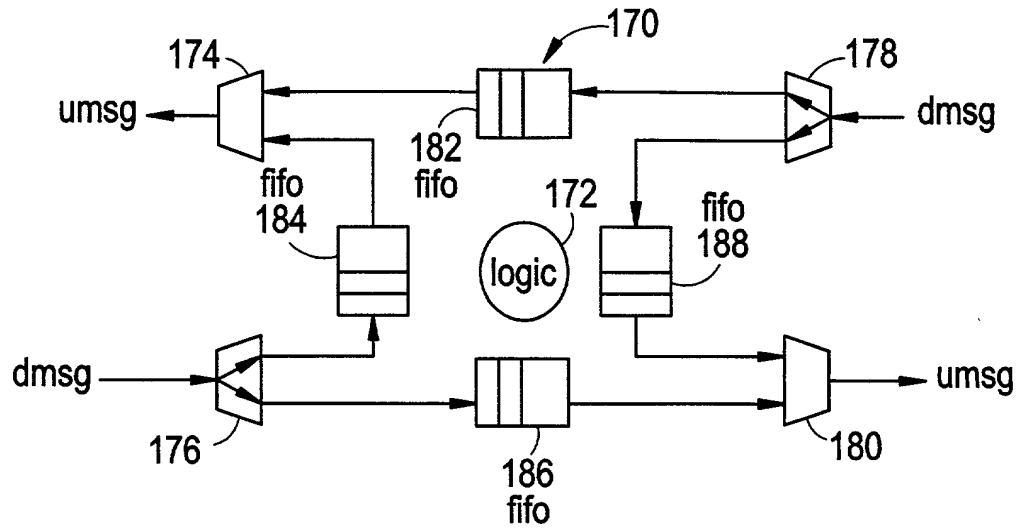


FIG. 18

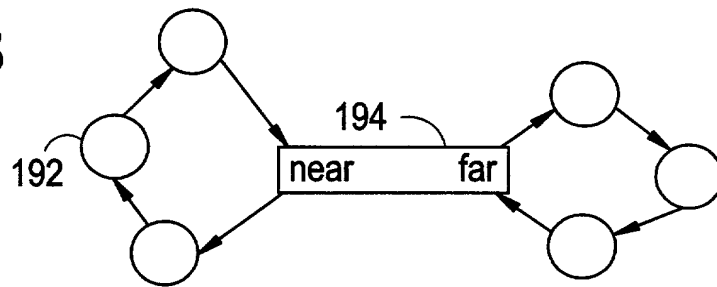


FIG. 19

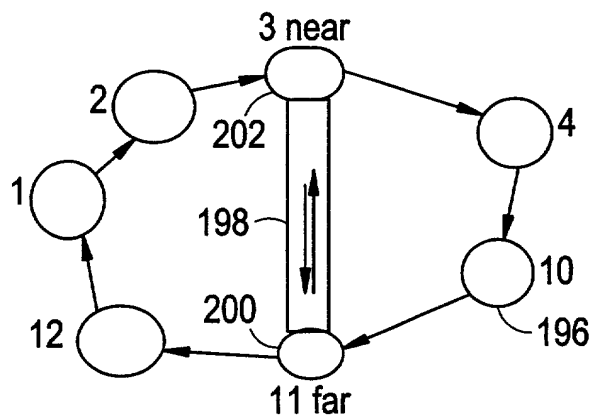


FIG. 20

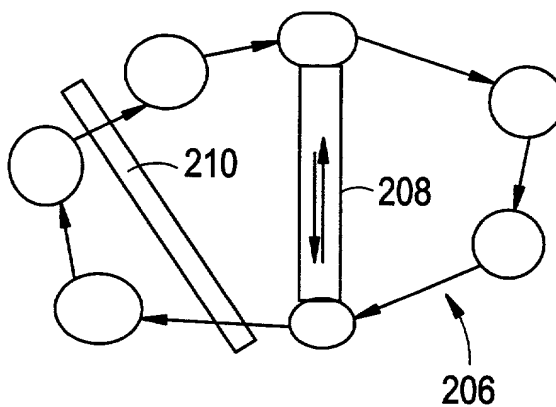


FIG. 21

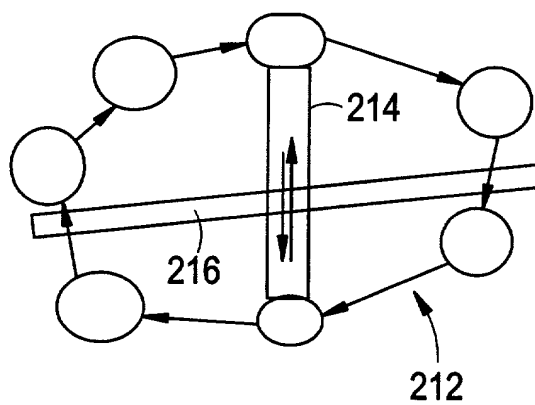


FIG. 22

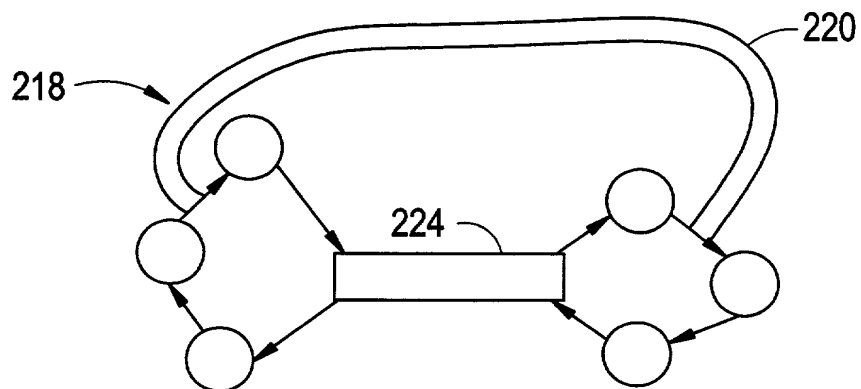


FIG. 23

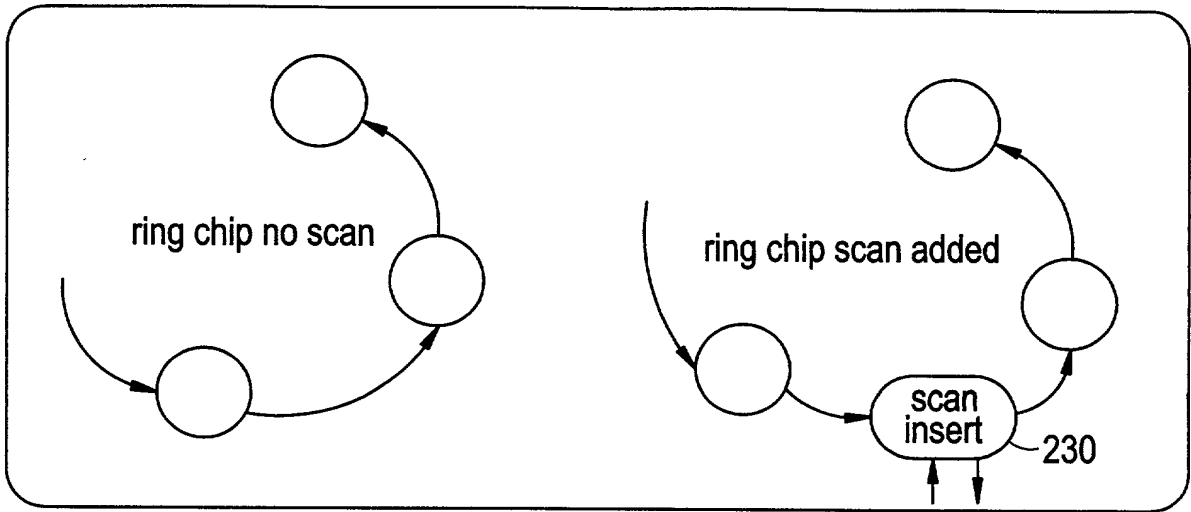


FIG. 24

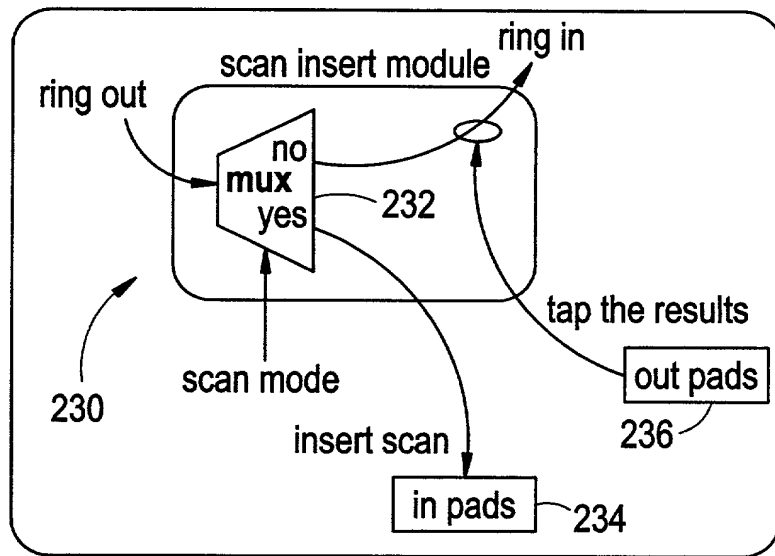


FIG. 25

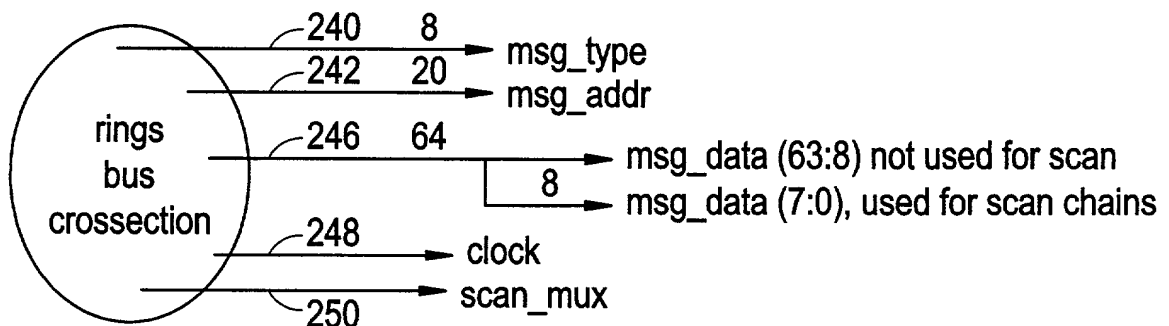


FIG. 26

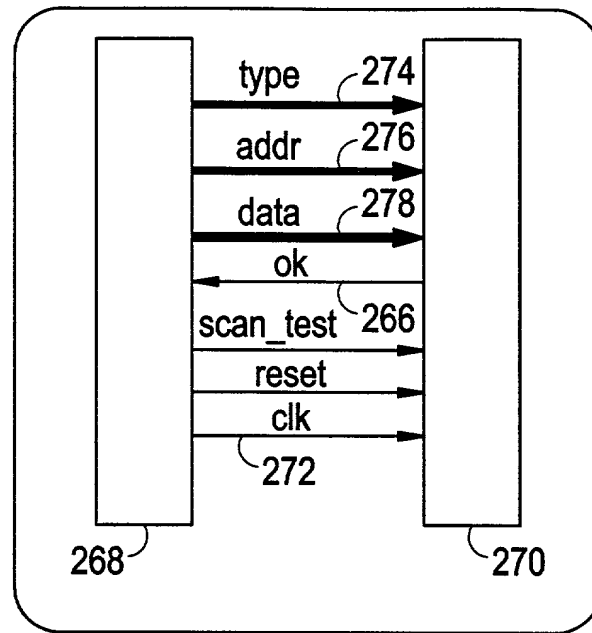


FIG. 27

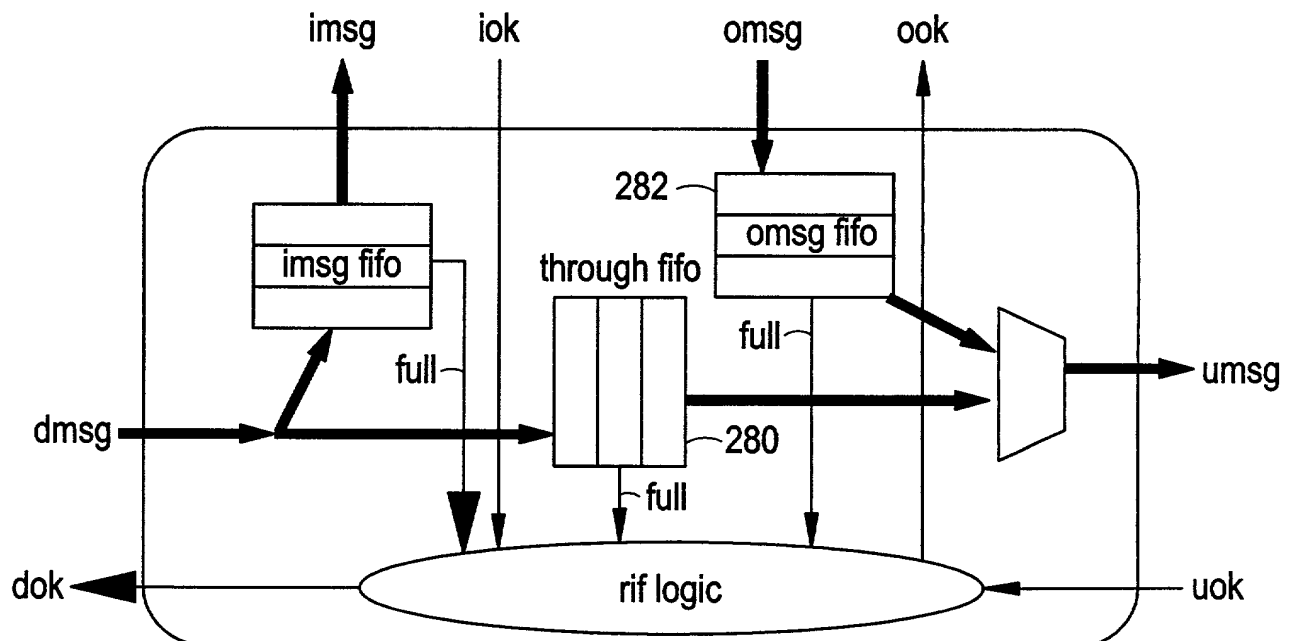


FIG. 28

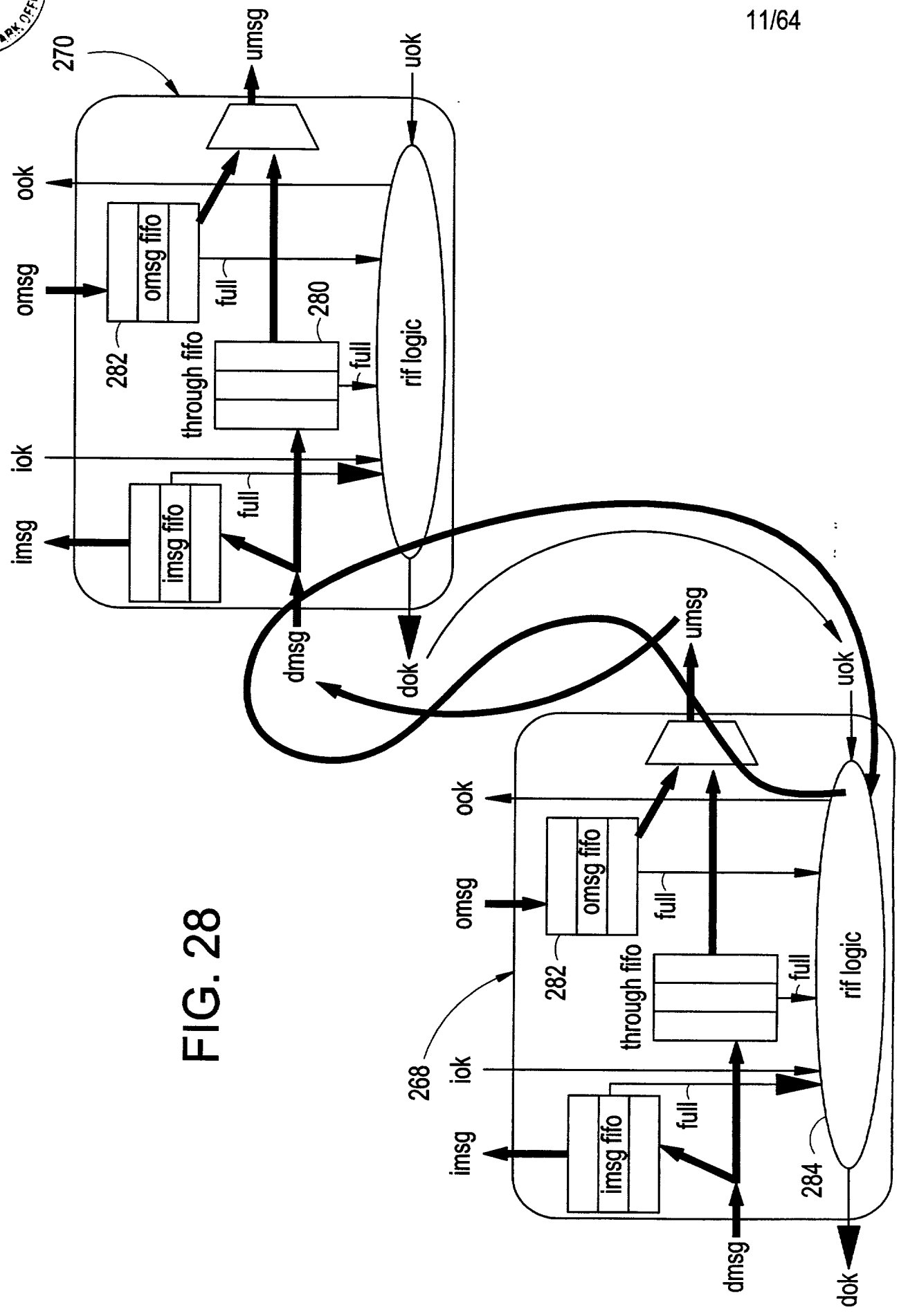


FIG. 29

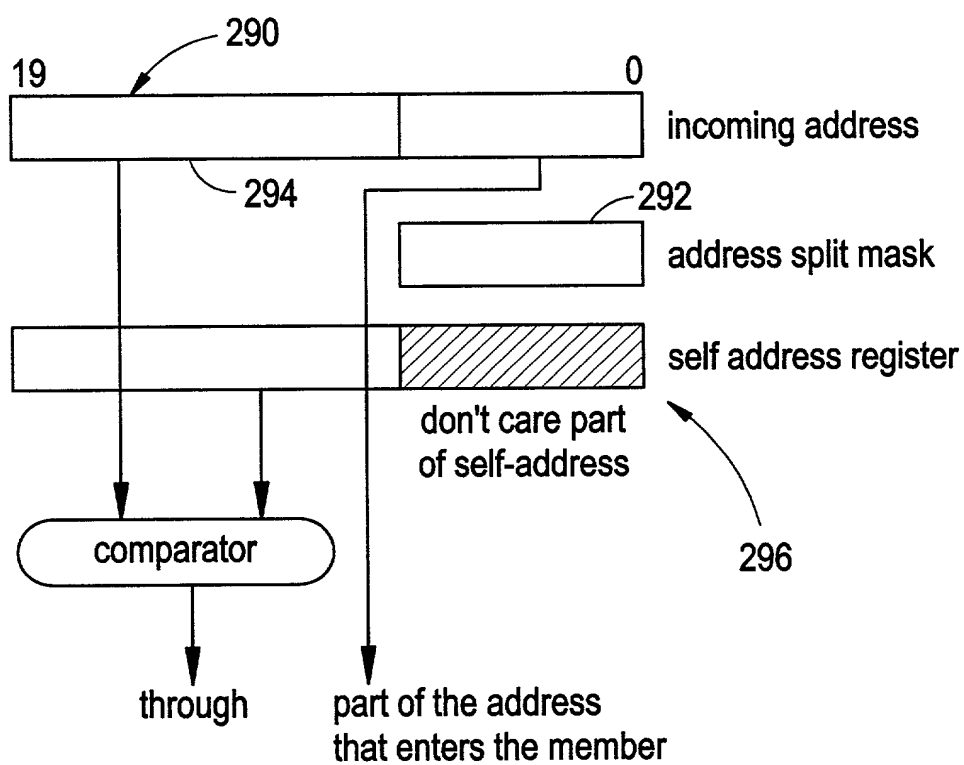


FIG. 30

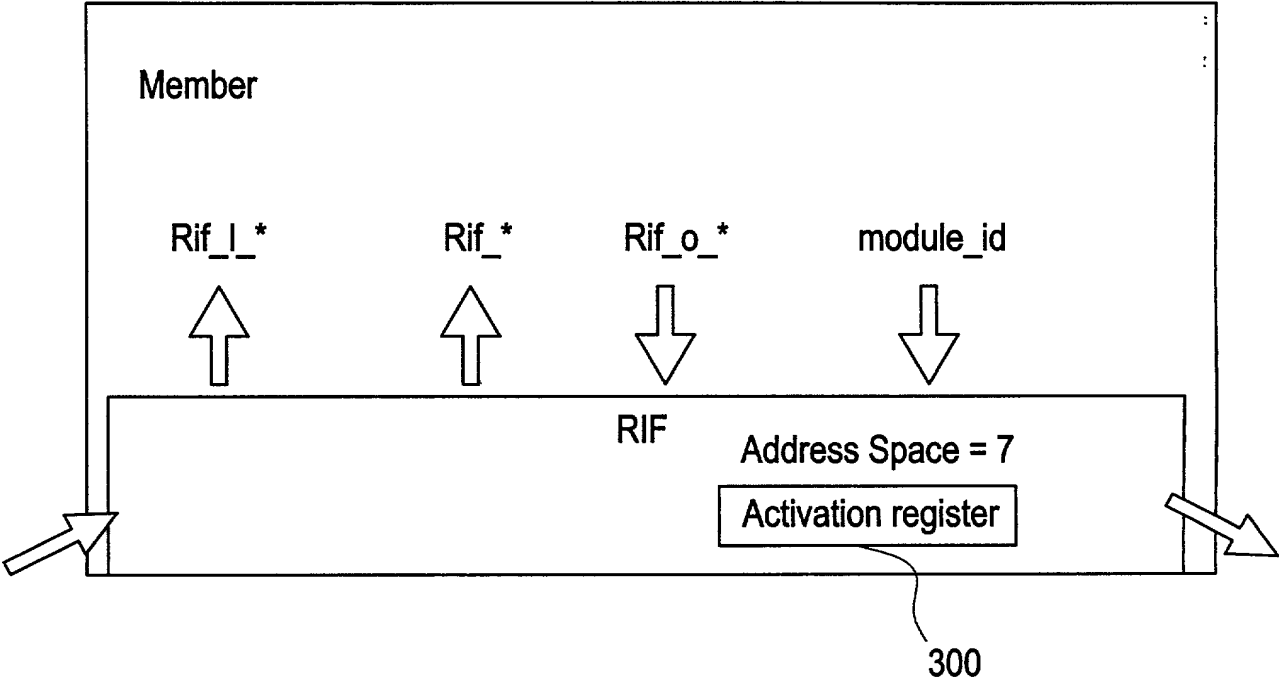


FIG. 31

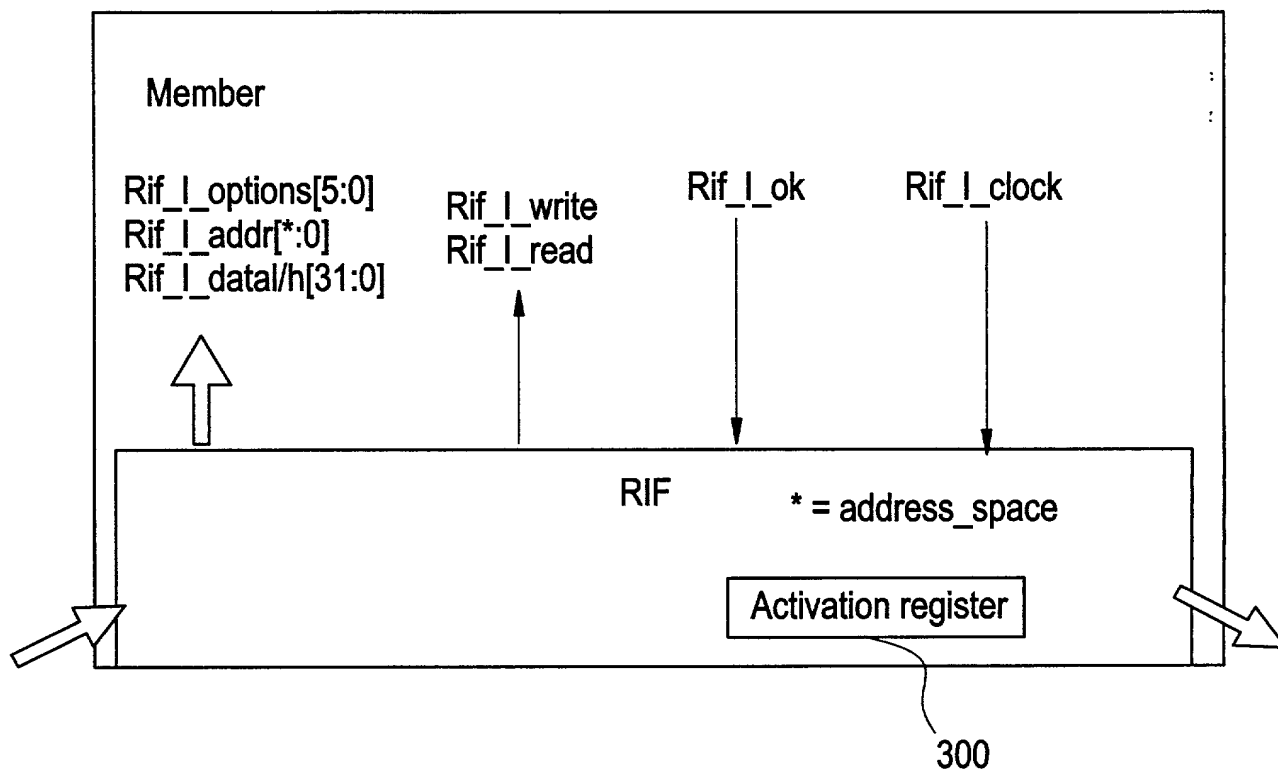


FIG. 32

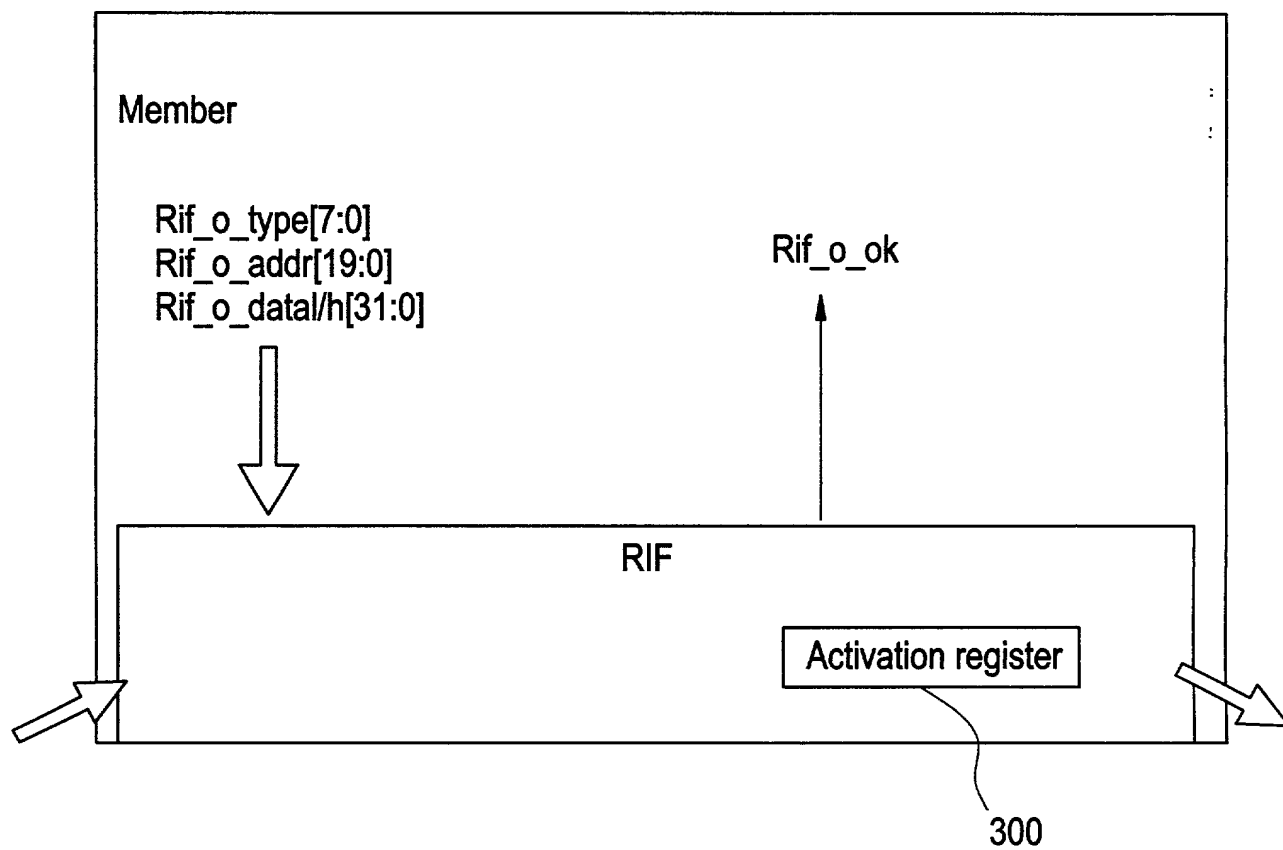


FIG. 33

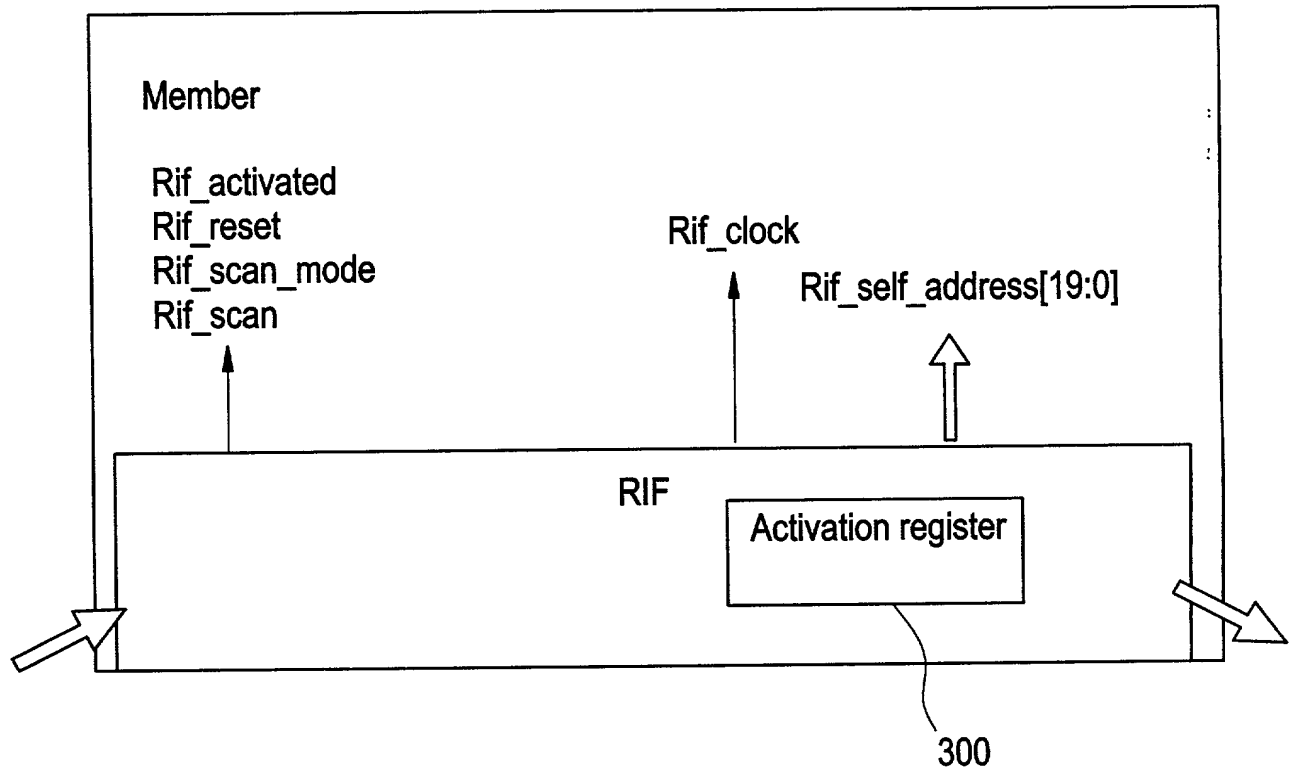


FIG. 34

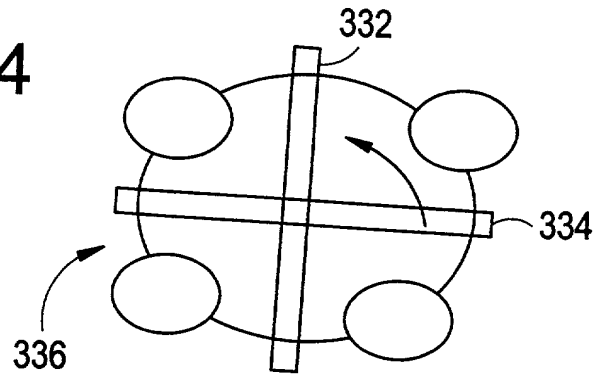


FIG. 35

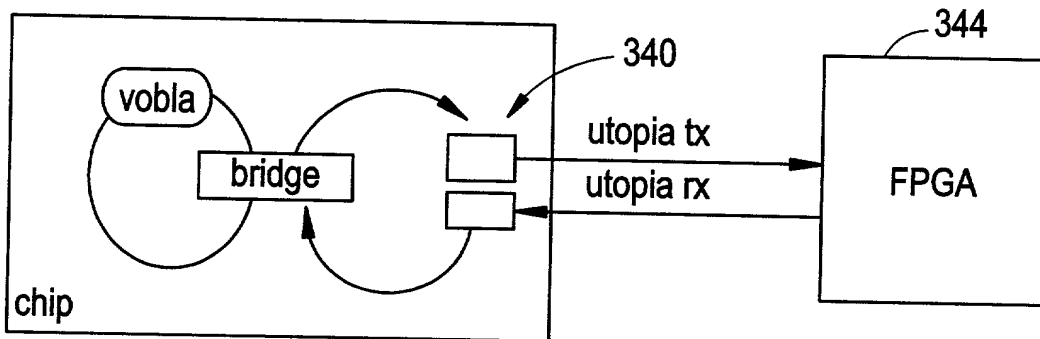


FIG. 36

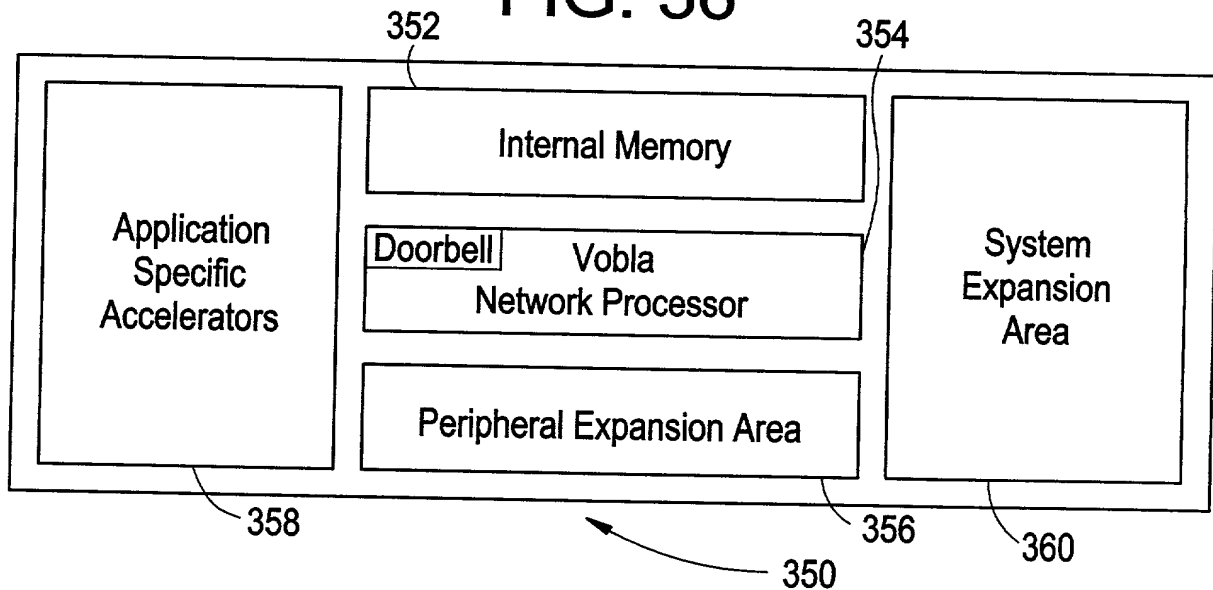
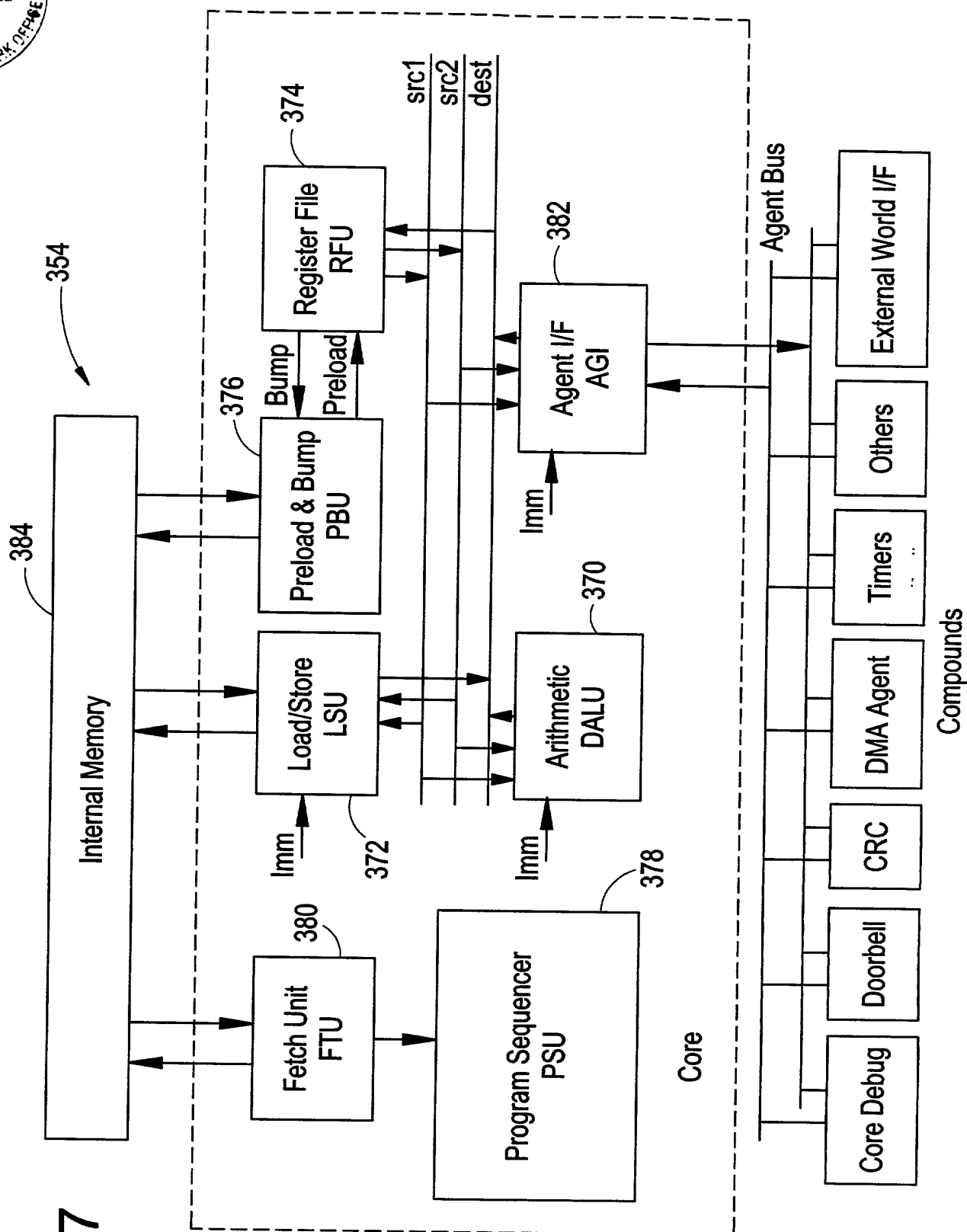


FIG. 37



Task_X

Task_Y

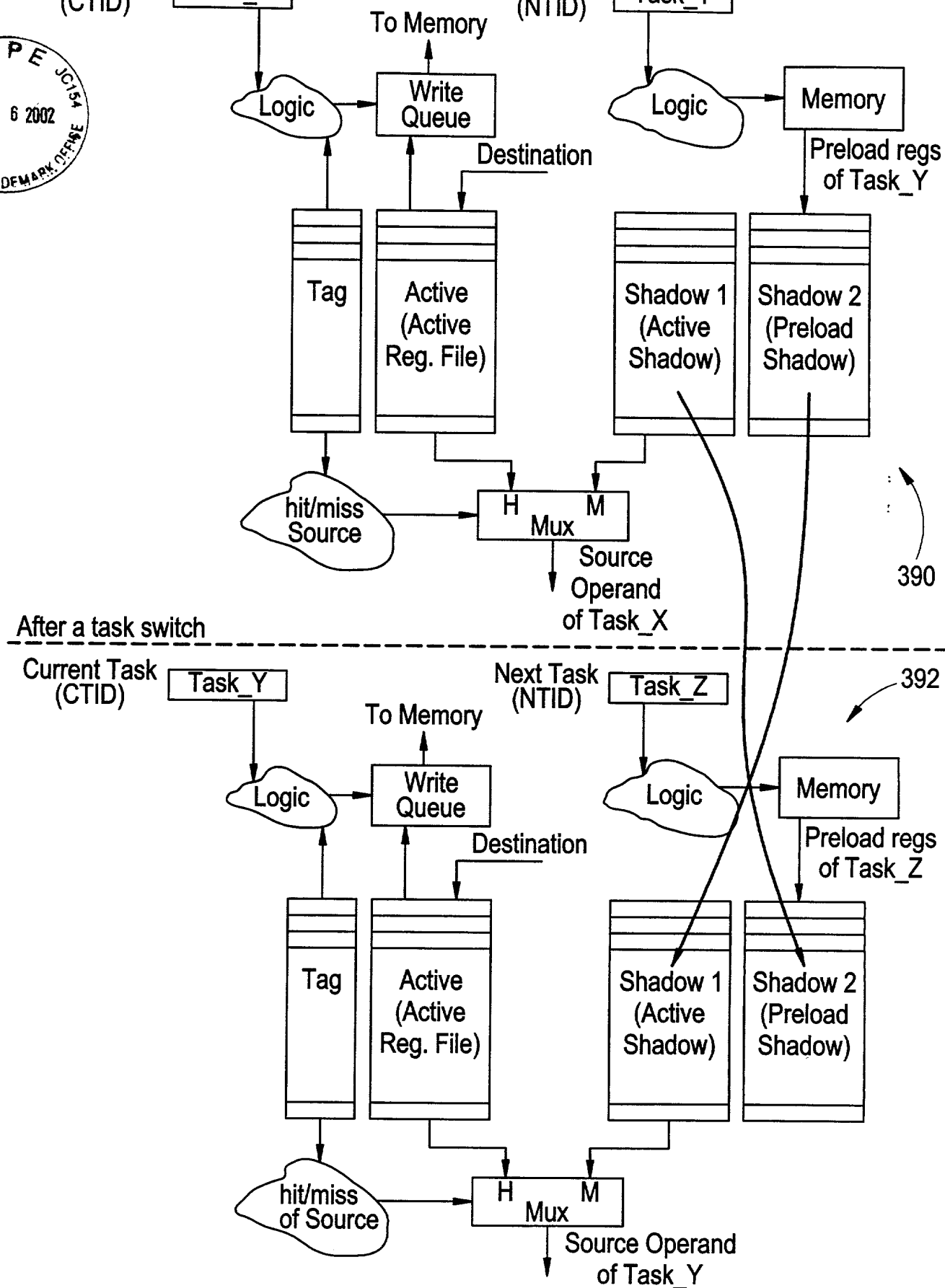


FIG. 39

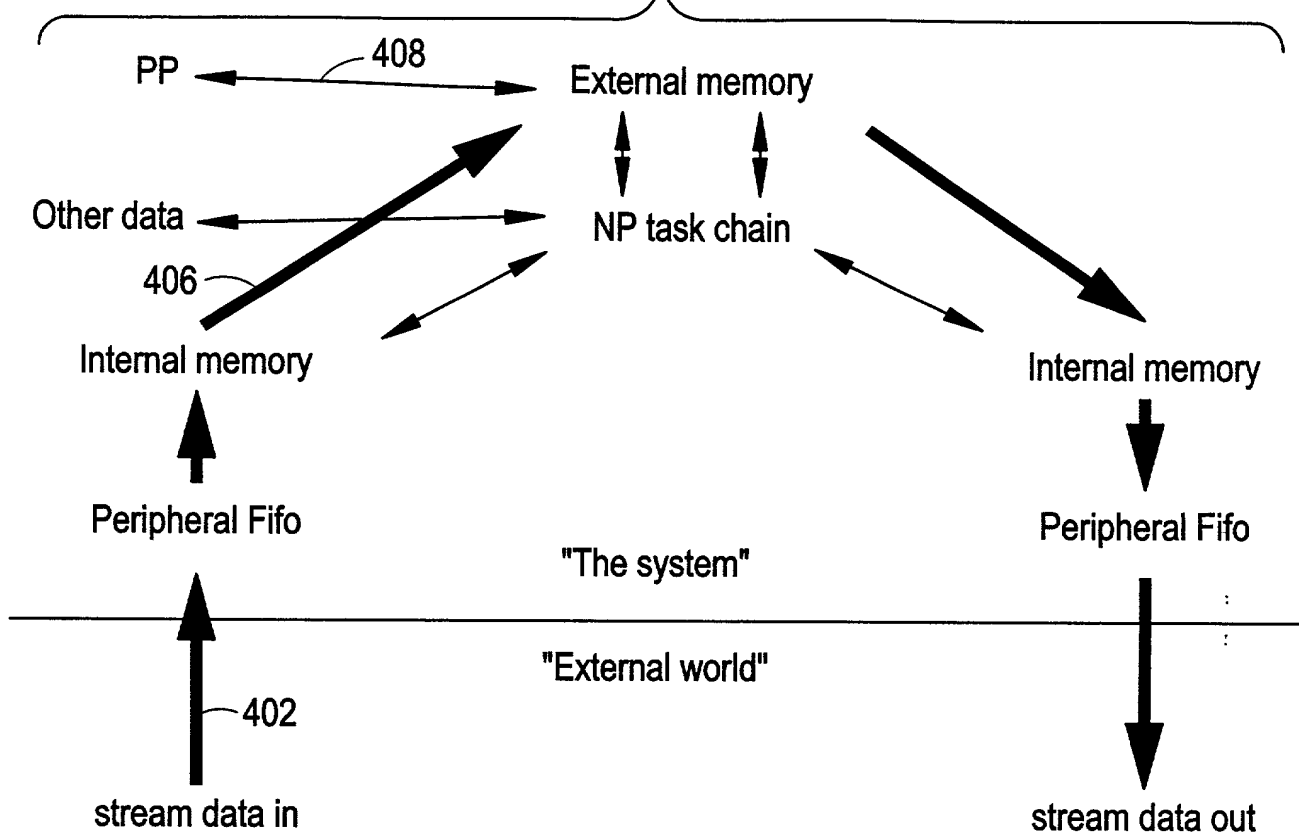


FIG. 40

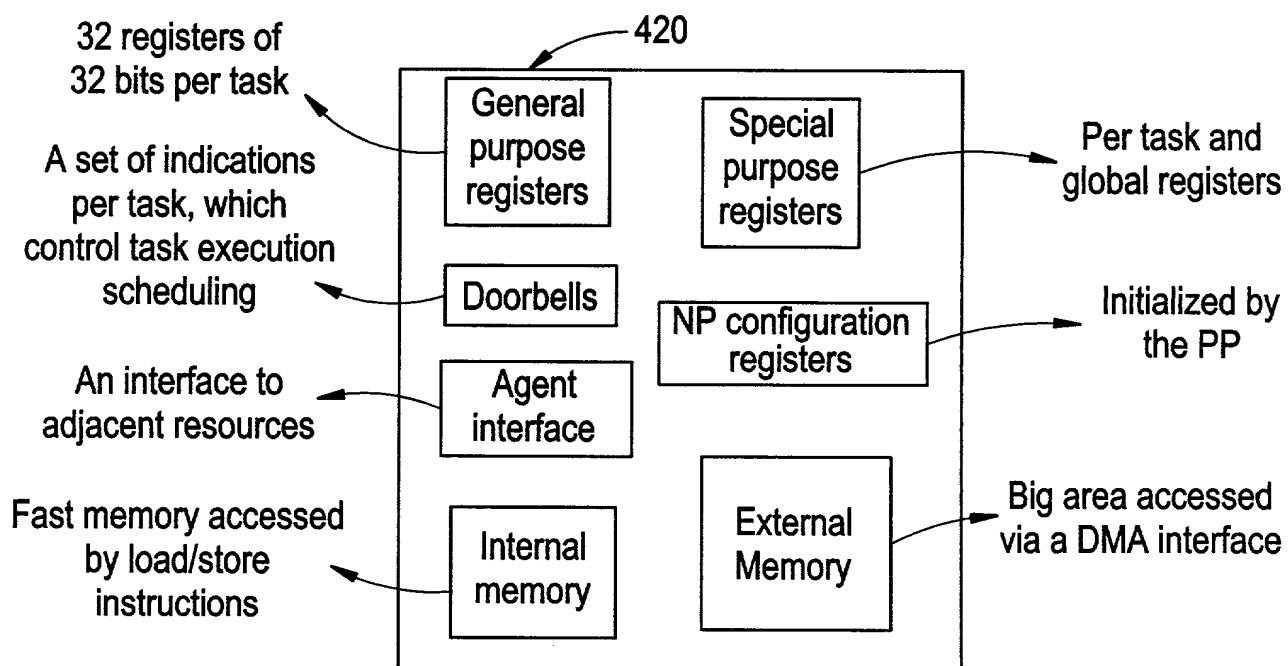
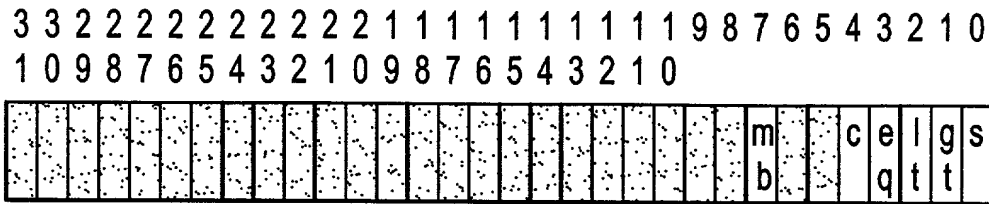


FIG. 41

R1 register



s - sticky bit
 eq - equal/zero
 lt - less then/negative
 gt - greater then/positive
 c - carry
 mb - reflection of the RAM mult-reader busy indication

430

FIG. 42

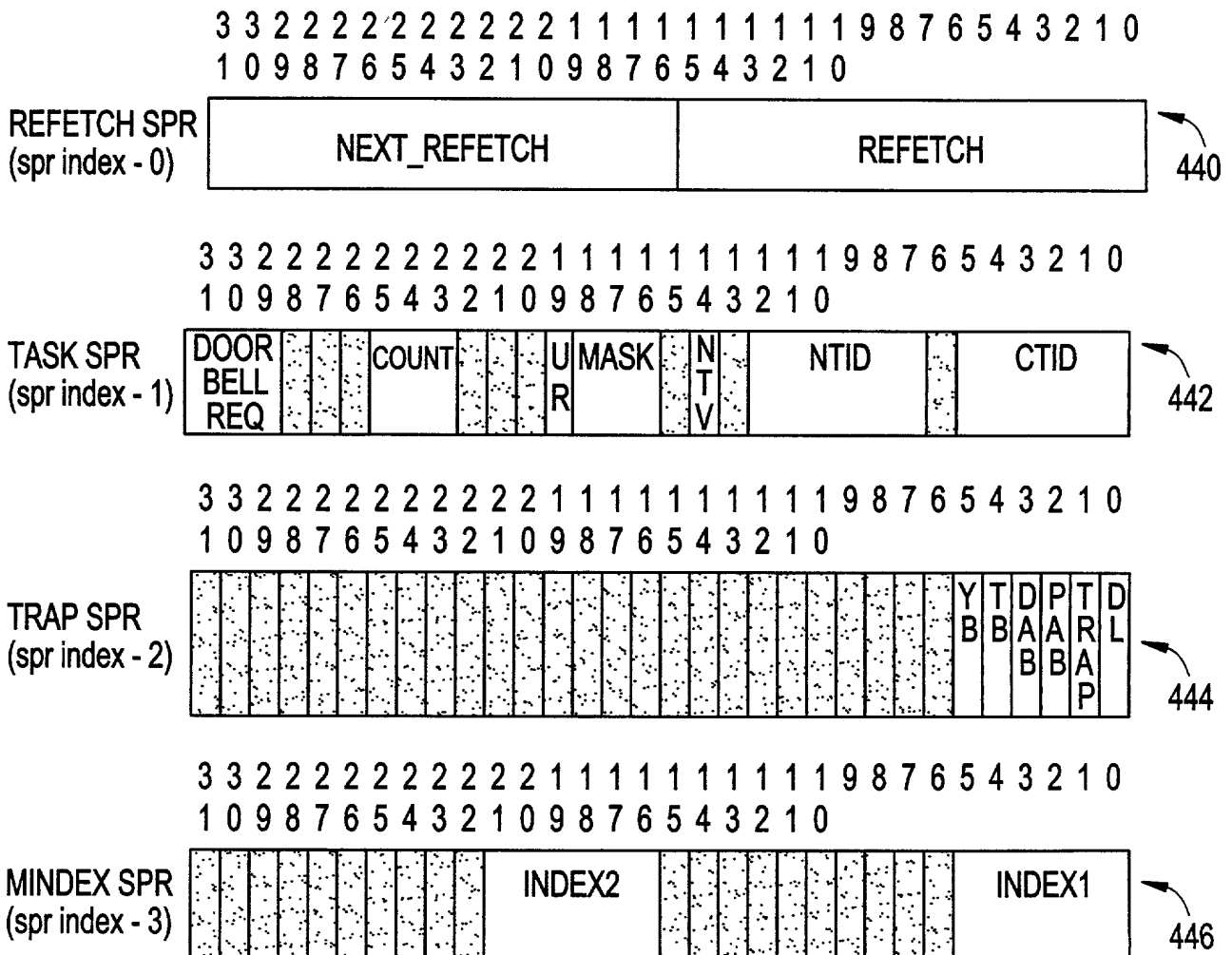


FIG. 43

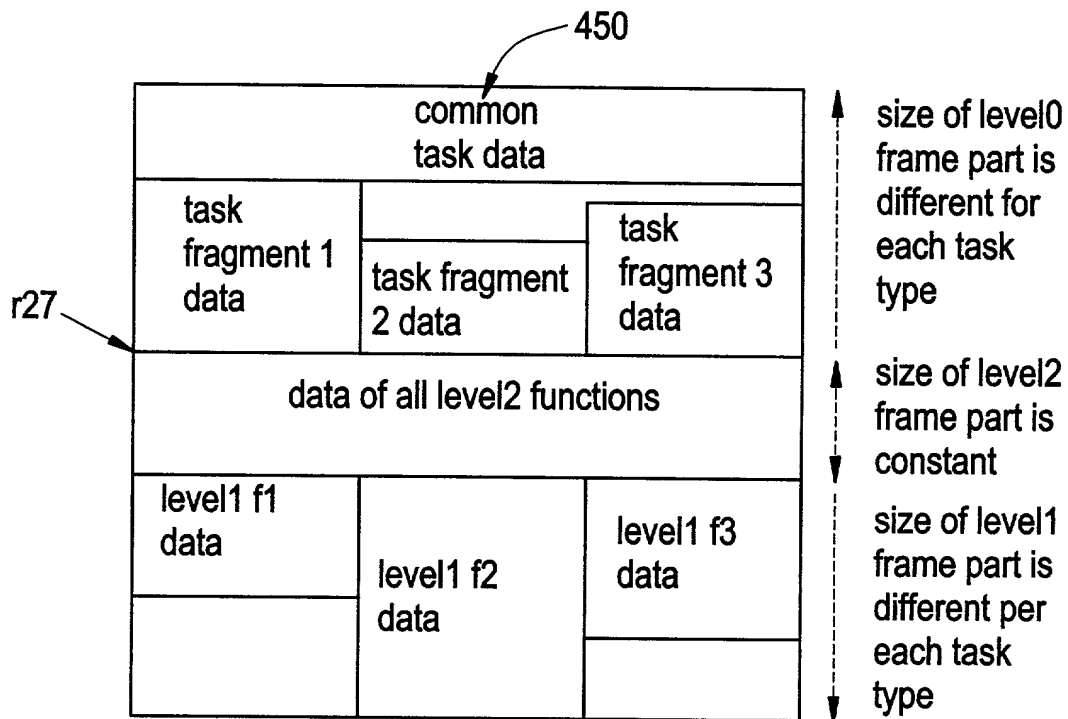


FIG. 44

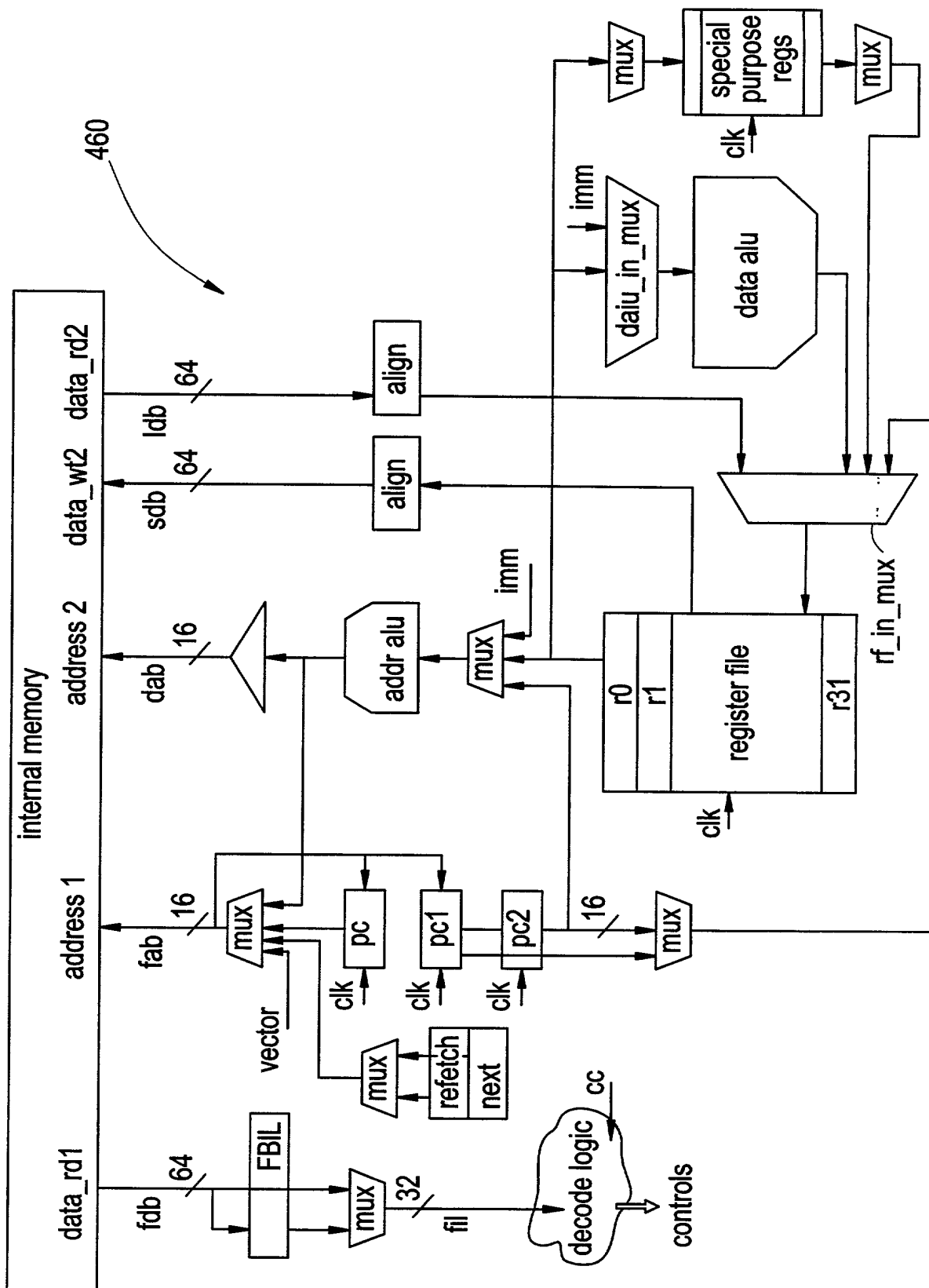
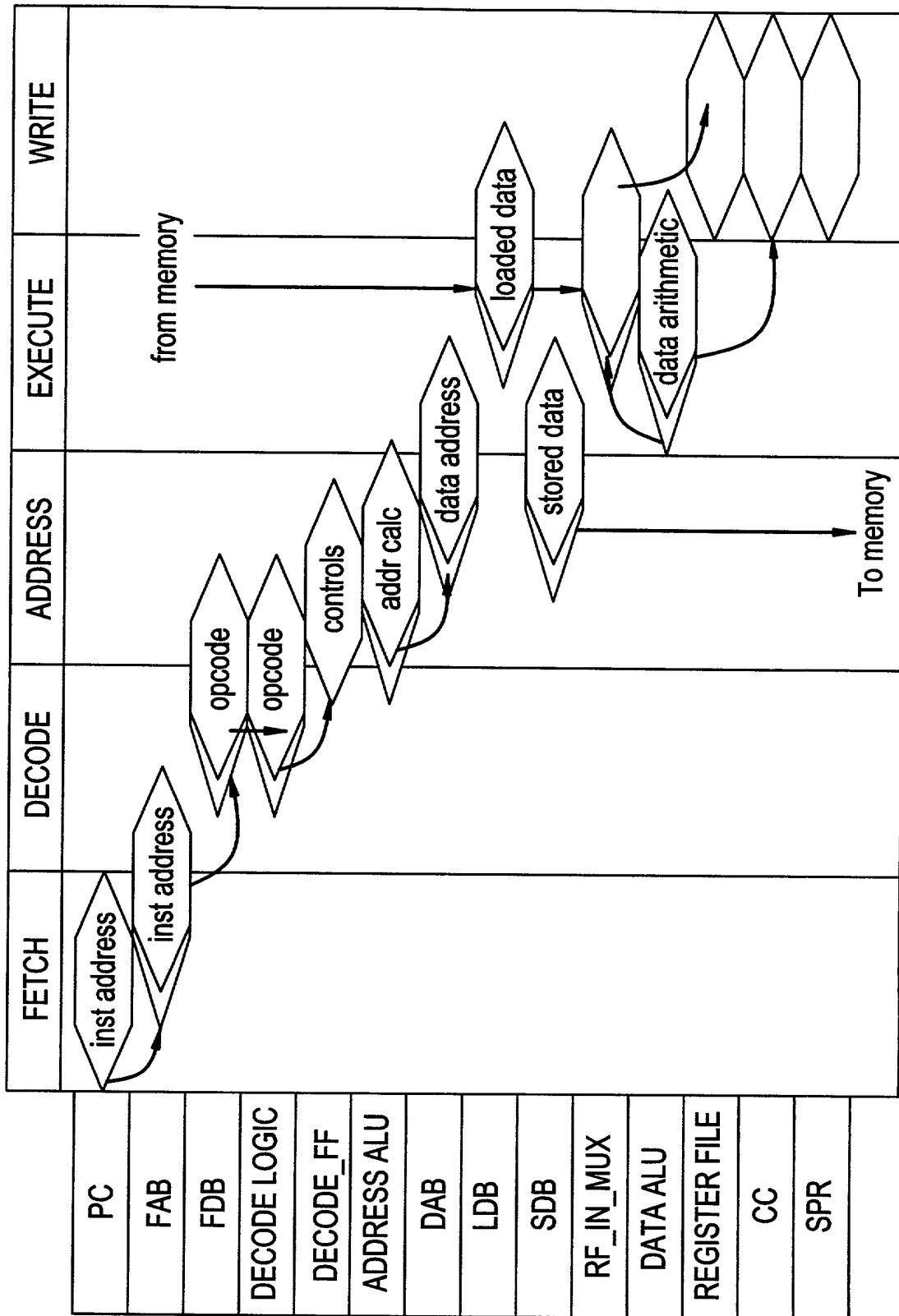




FIG. 45



480



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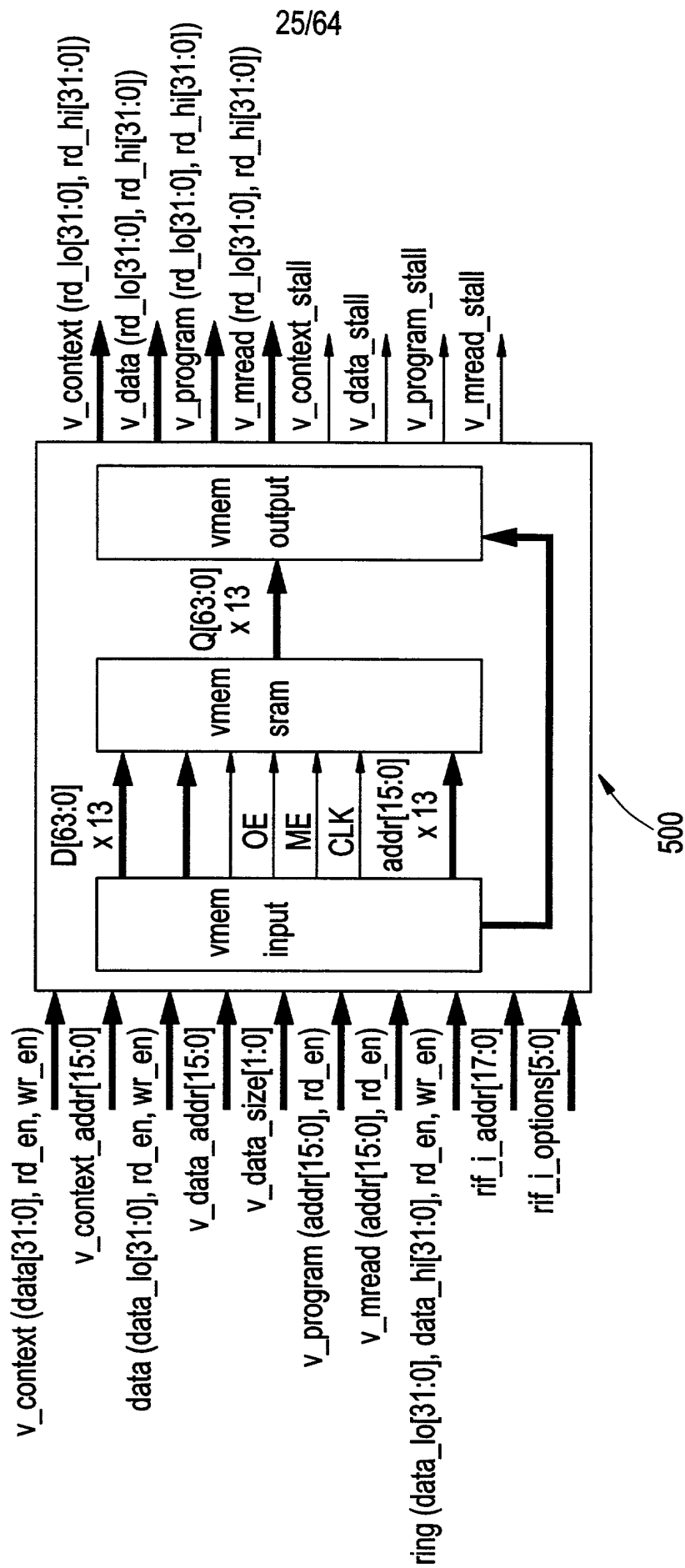


FIG. 47

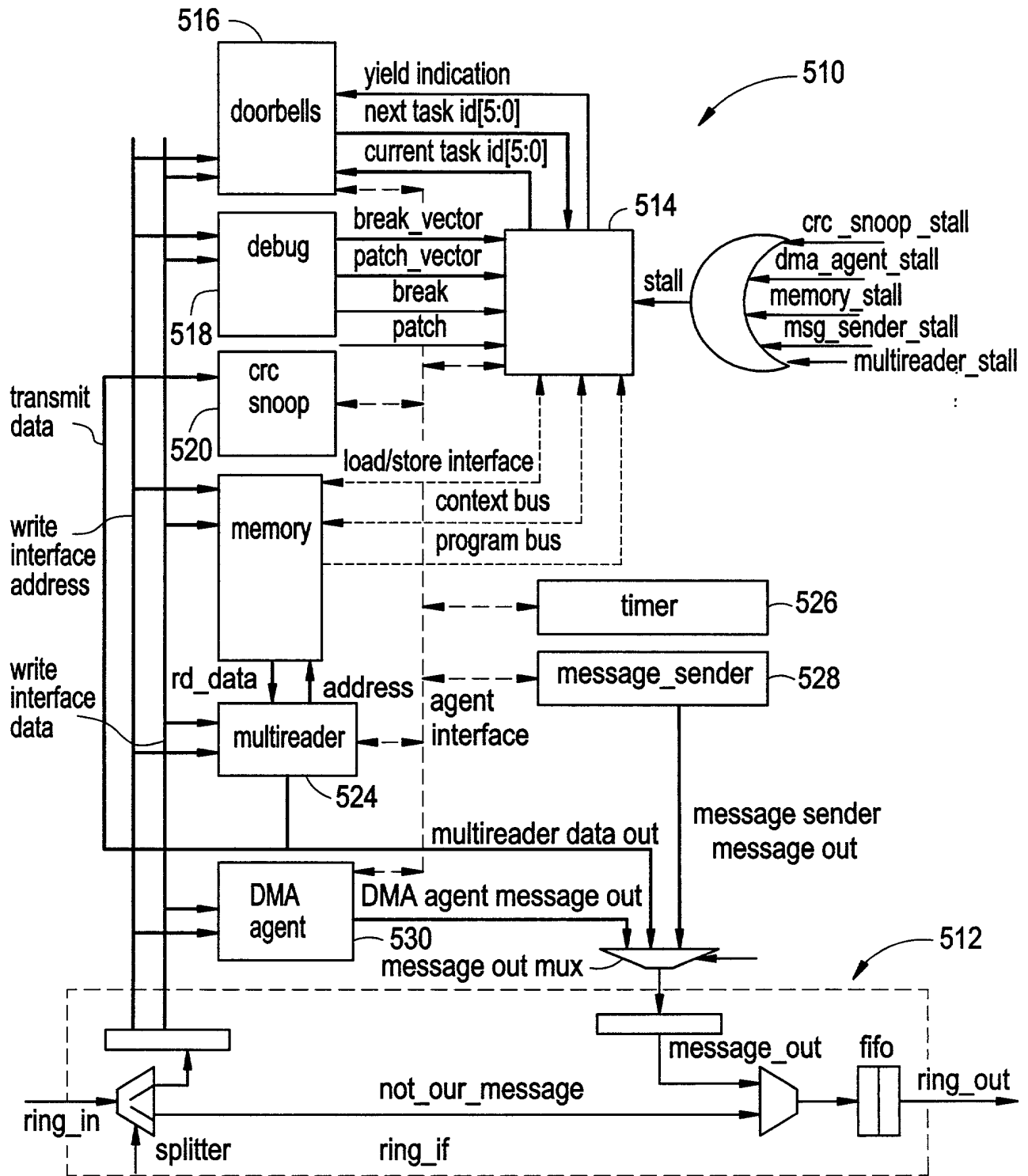


FIG. 48

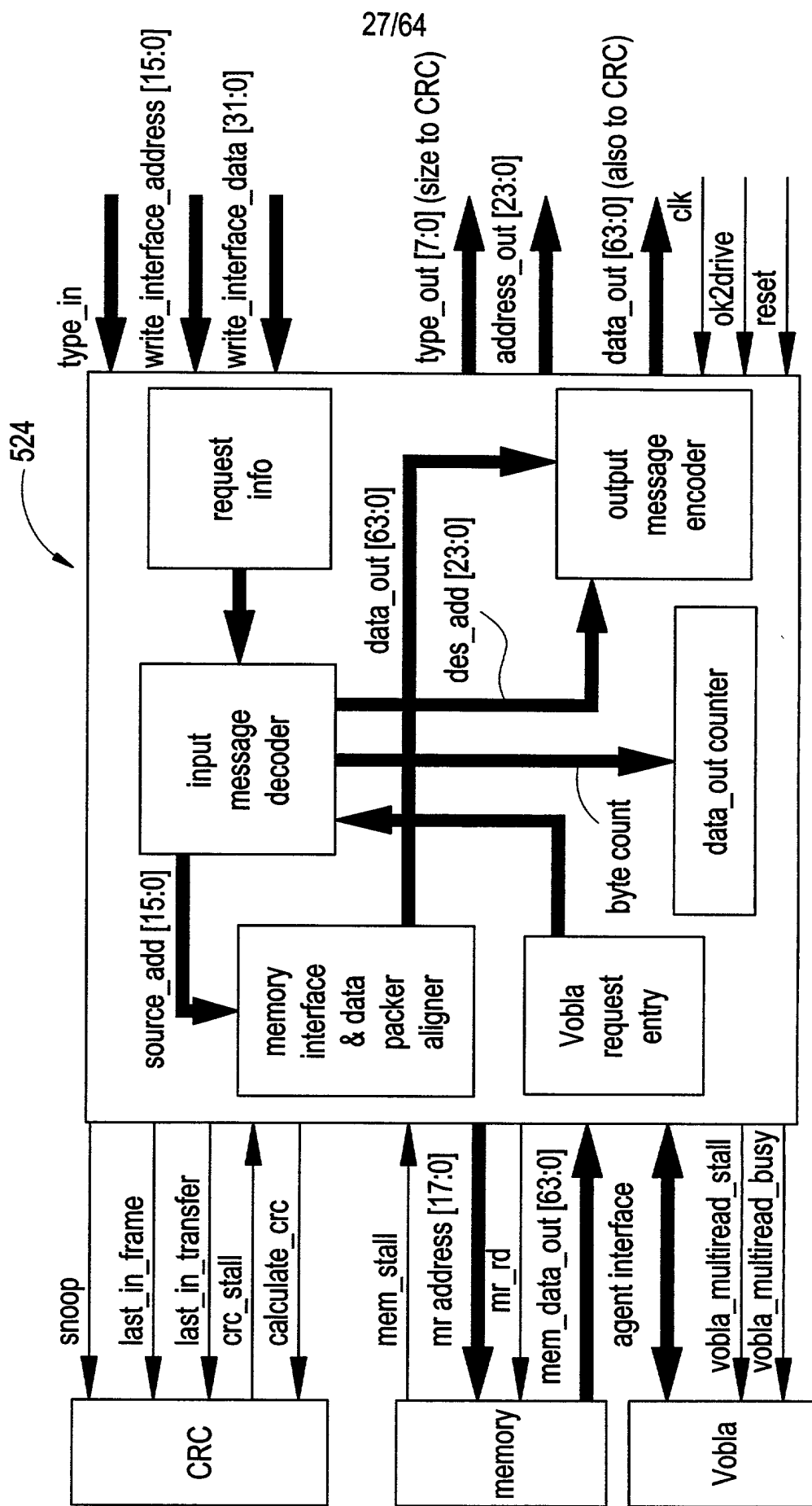


FIG. 49

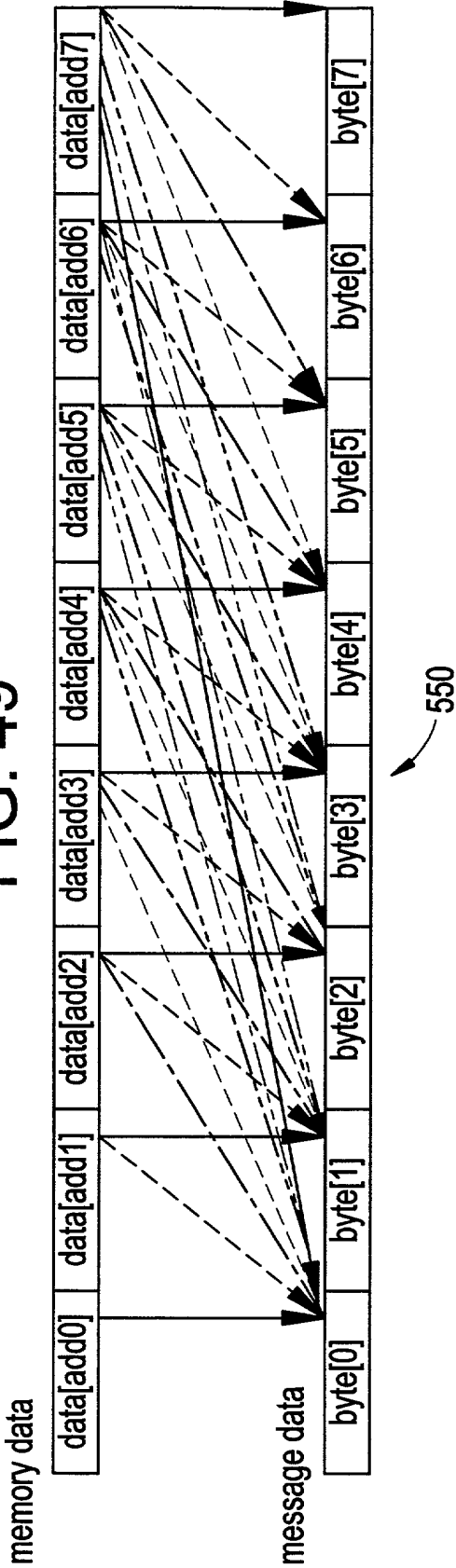
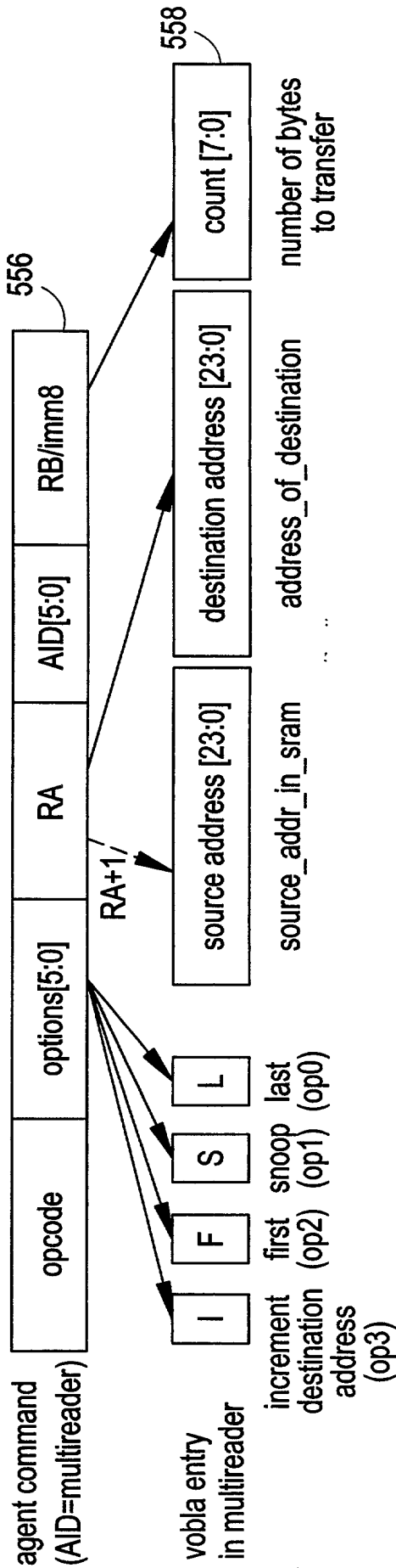


FIG. 50



20250703 09:49:00

FIG. 51

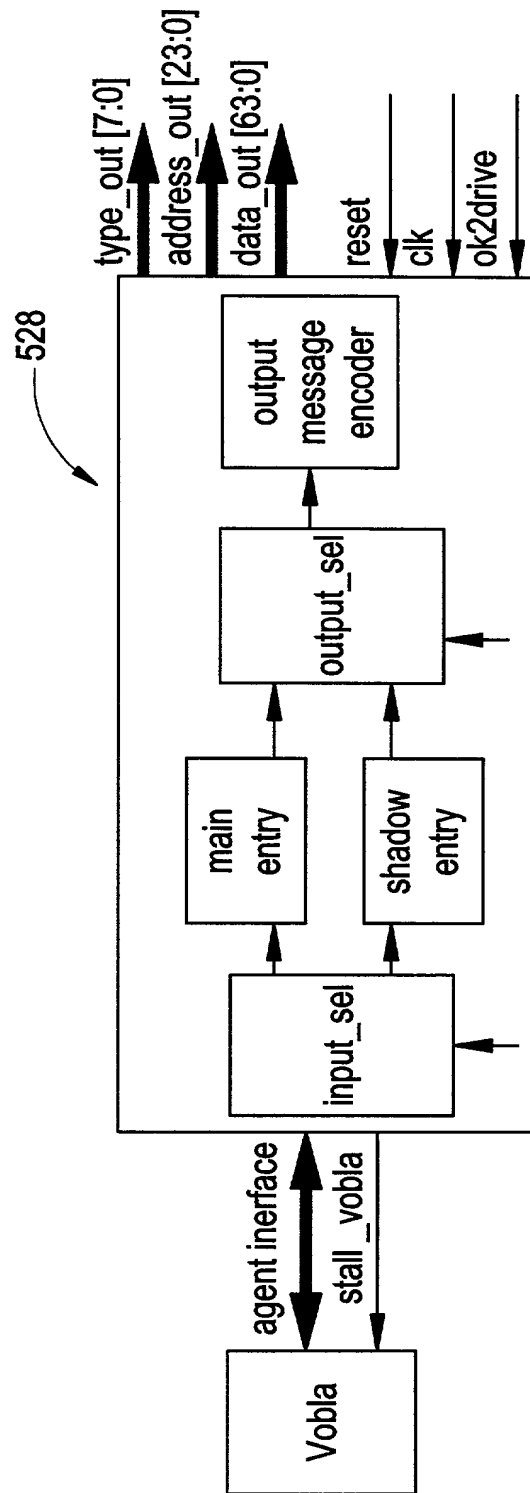


FIG. 52

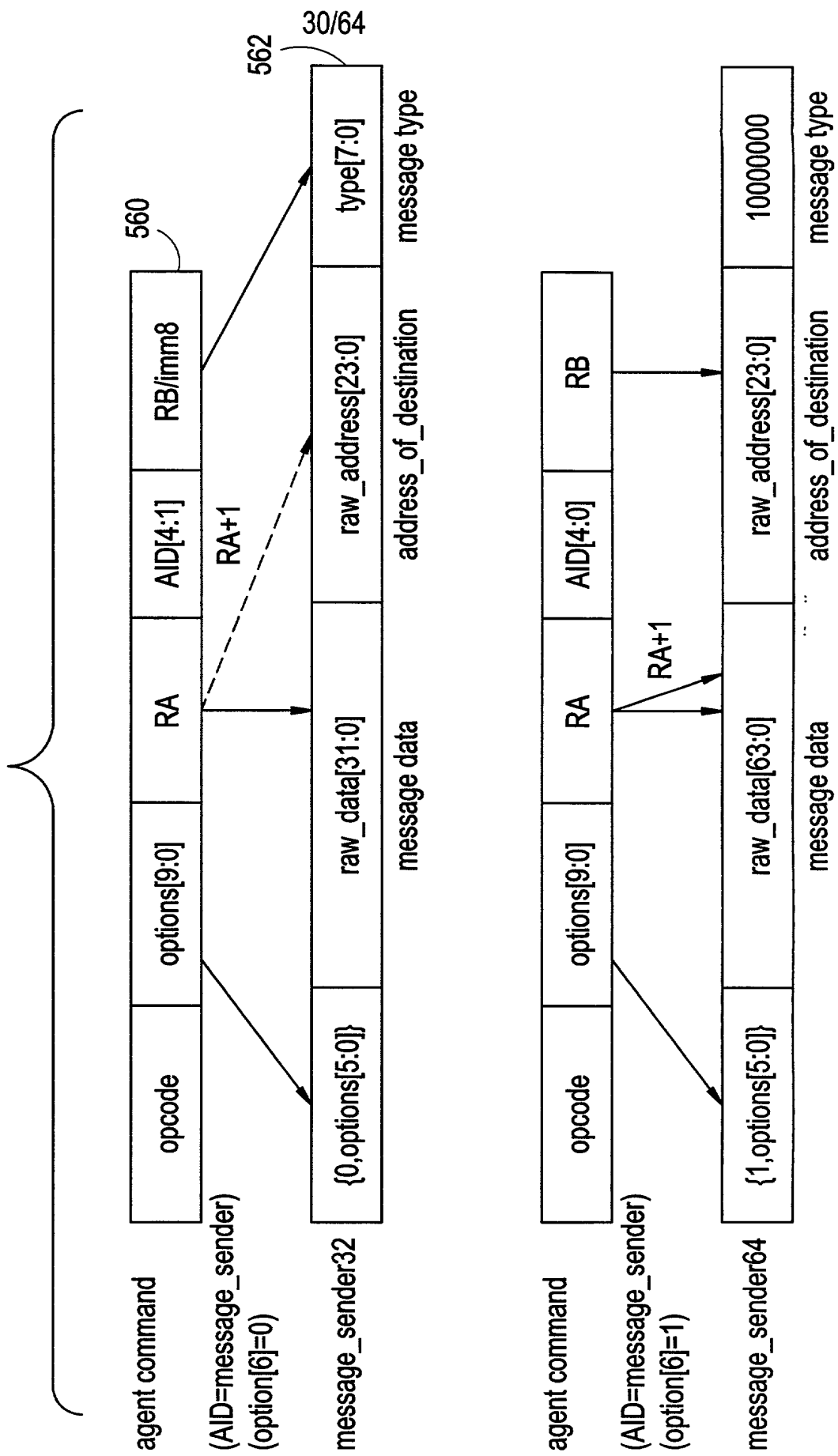


FIG. 53

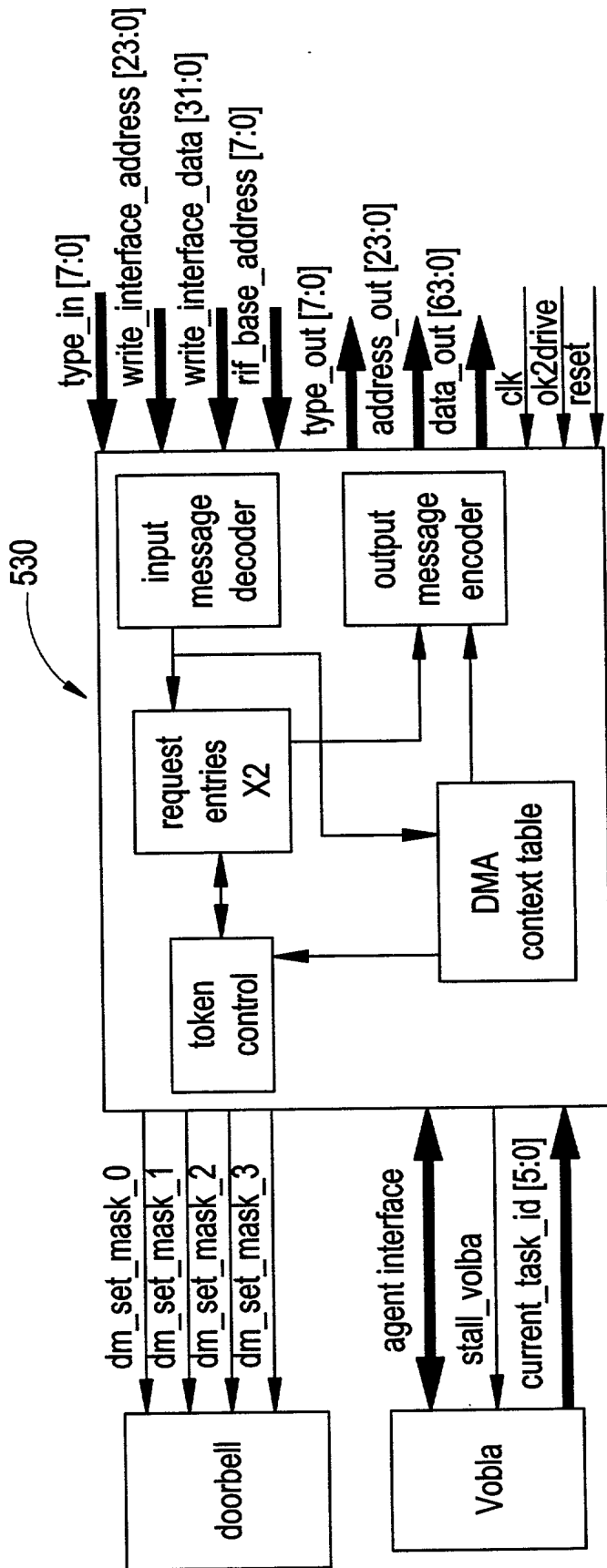


Figure 1 illustrates the DMA request entry format. The entry is a 32/64-bit structure. The top 16 bits (labeled 576) contain the opcode, options[10:0], RA, AID[4:0], and RB/imm8. The bottom 16 bits (labeled 578) contain the count[7:0]. The options field is further detailed with bits M, U, D, A, NA, and L. The RA field is labeled RA+1. The AID field is labeled AID[4:0]. The RB/imm8 field is labeled RB/imm8. The count field is labeled {count [7:0]}. The structure is divided into three main sections: dma request entry (M, U, D, A, NA, L), dram address (RA+1), and sram address (AID[4:0], RB/imm8). The count field is labeled number of bytes to transfer or address modifier.

FIG. 55

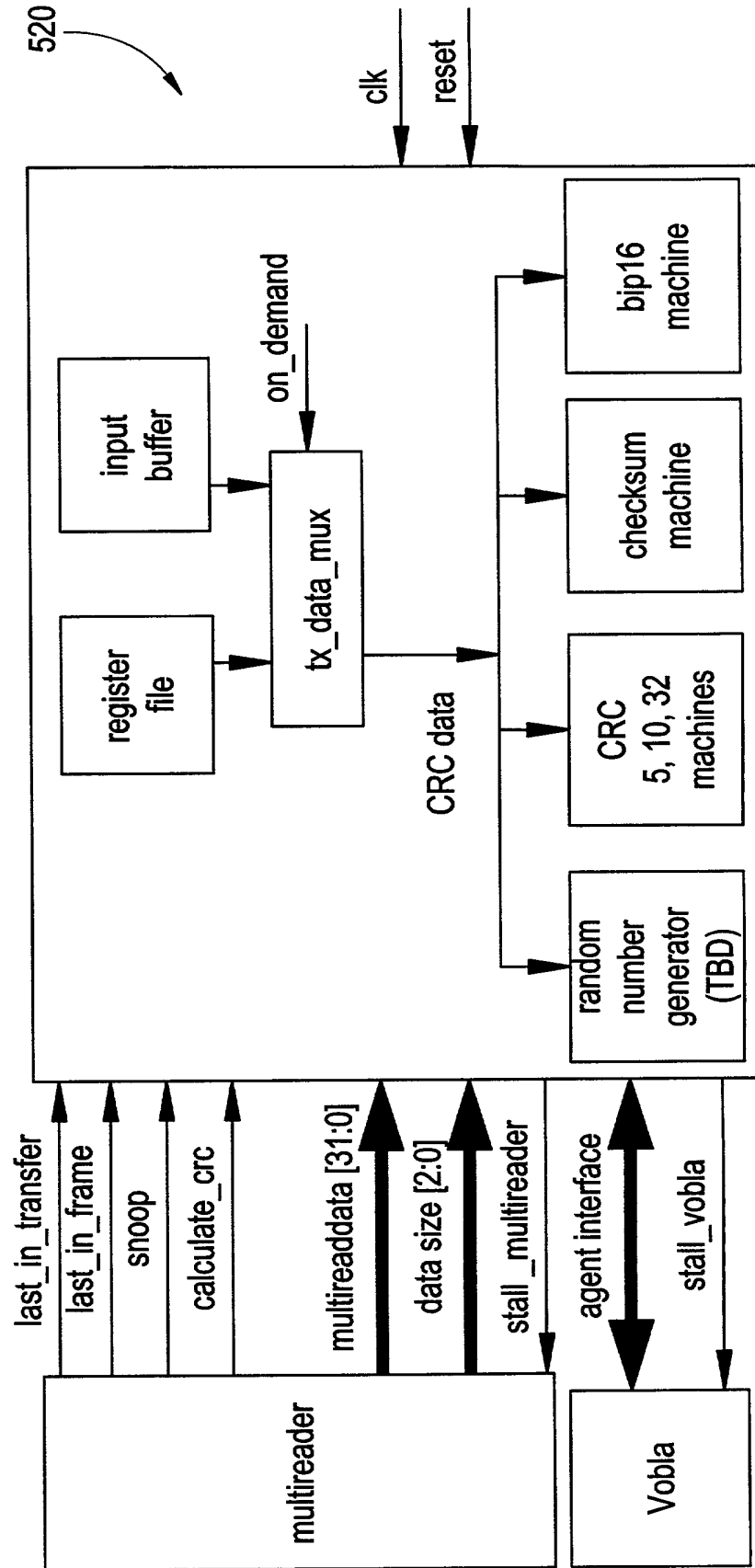




FIG. 56

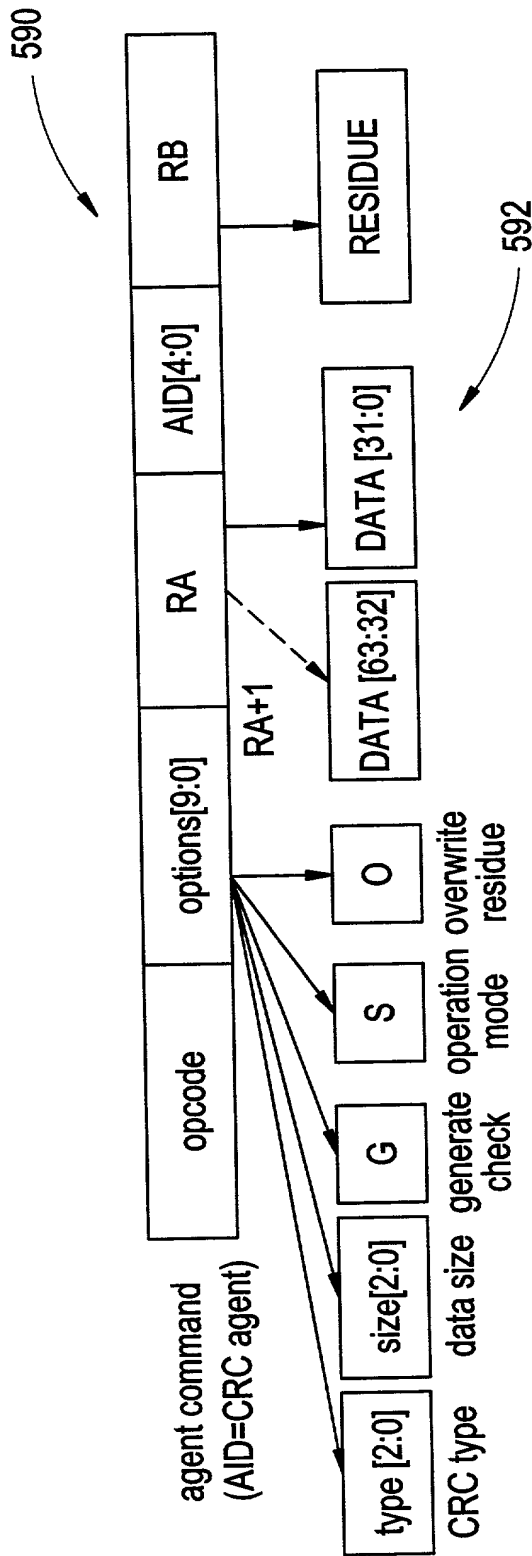


FIG. 57

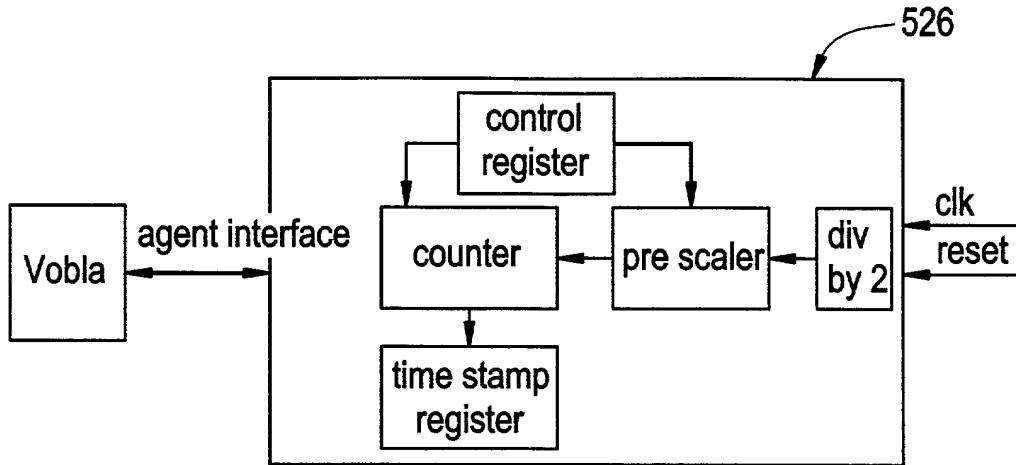


FIG. 58

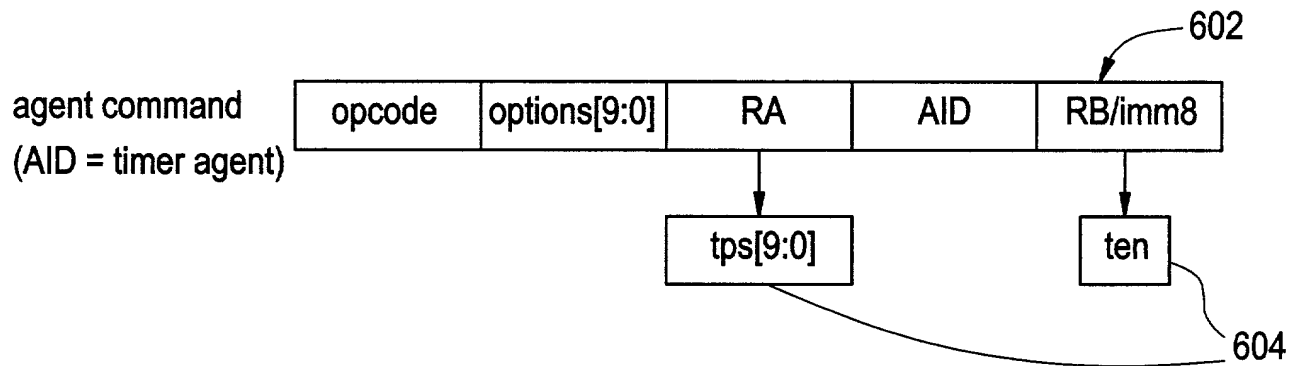


FIG. 59

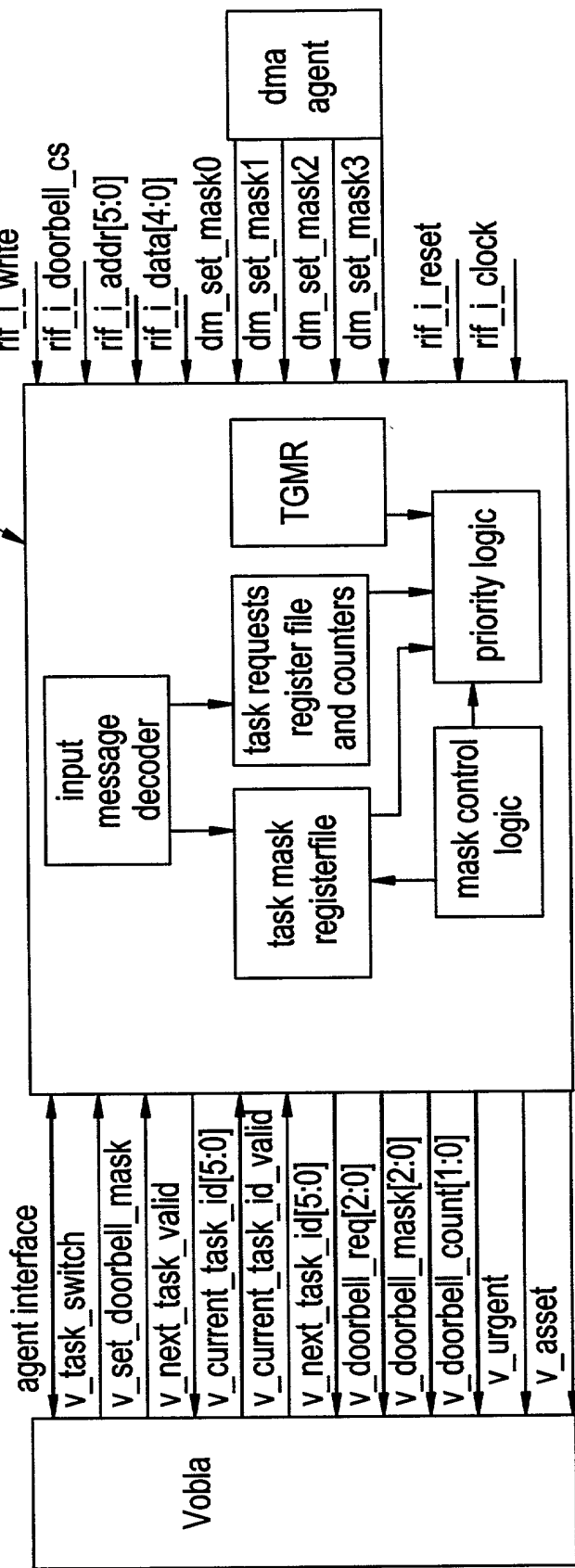


FIG. 60

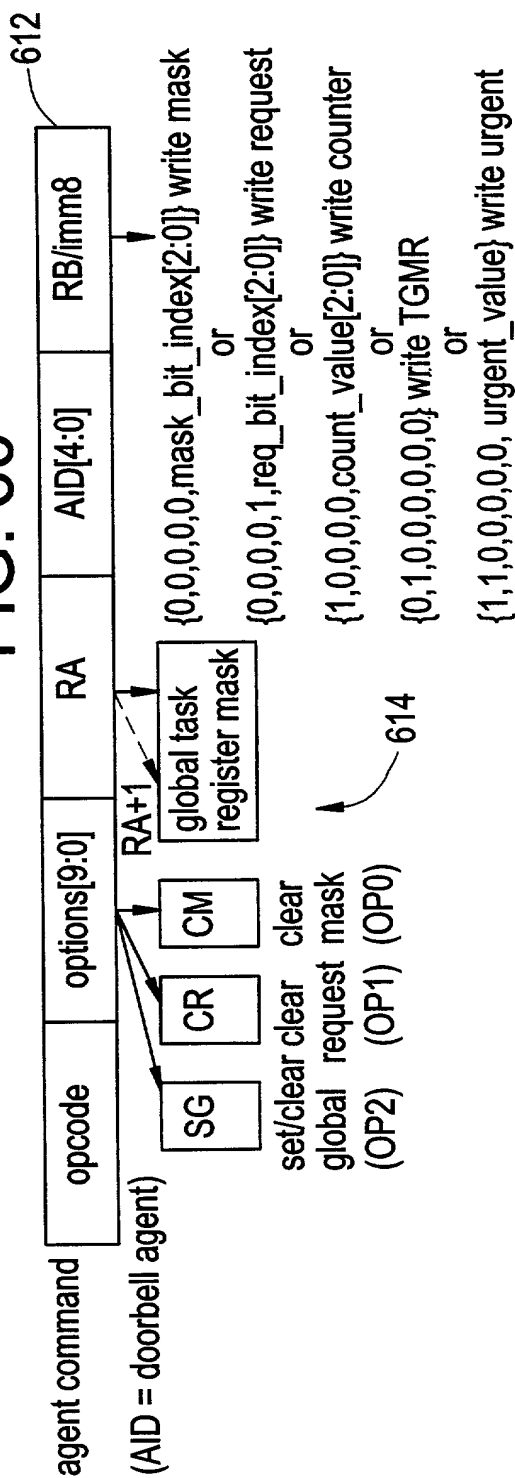
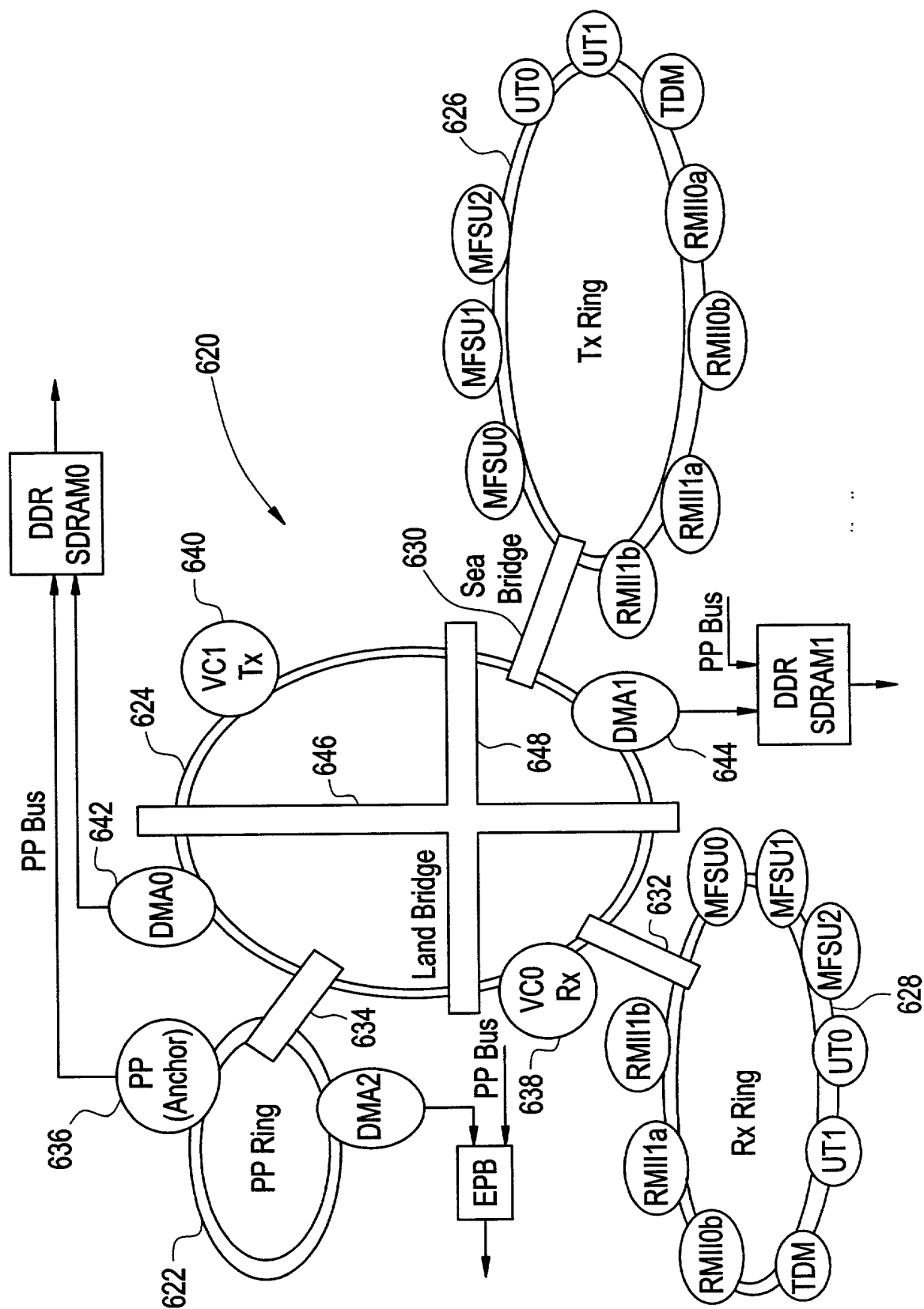


FIG. 61



2003260" 06649001

FIG. 62

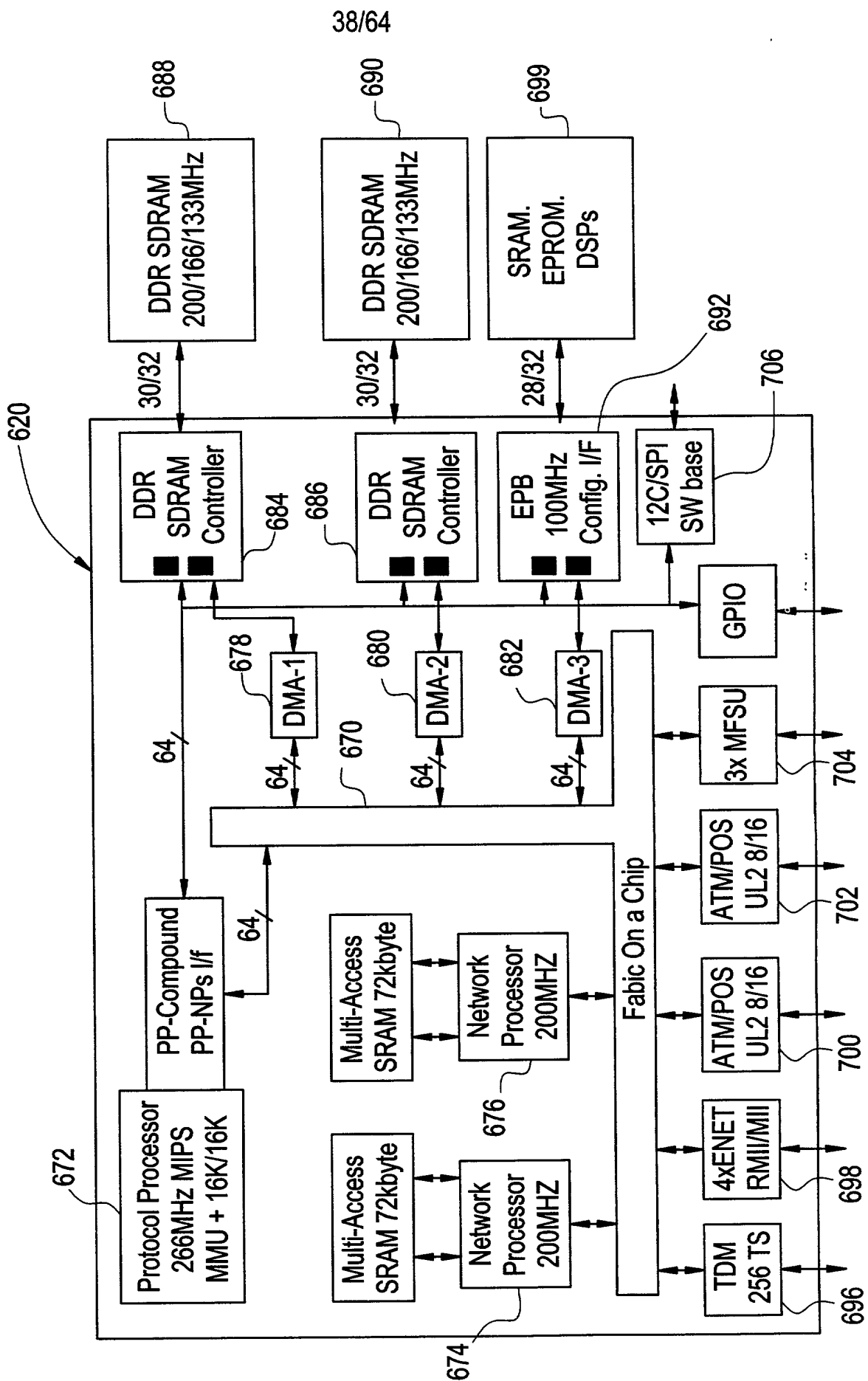


FIG. 63

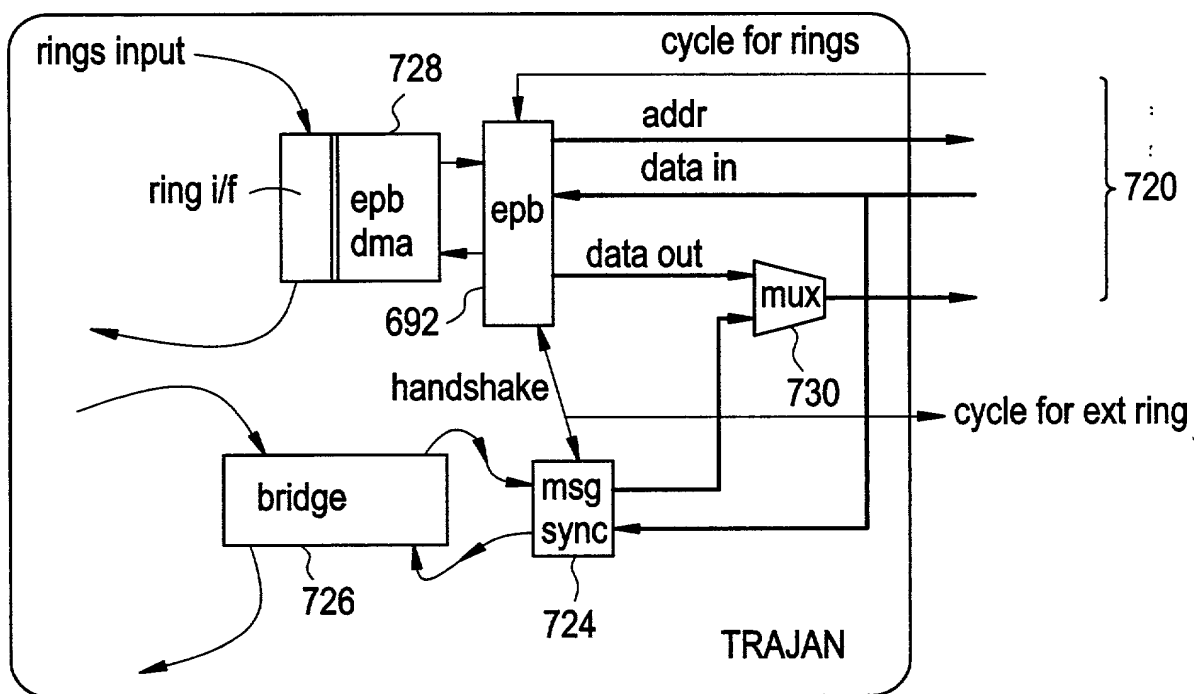
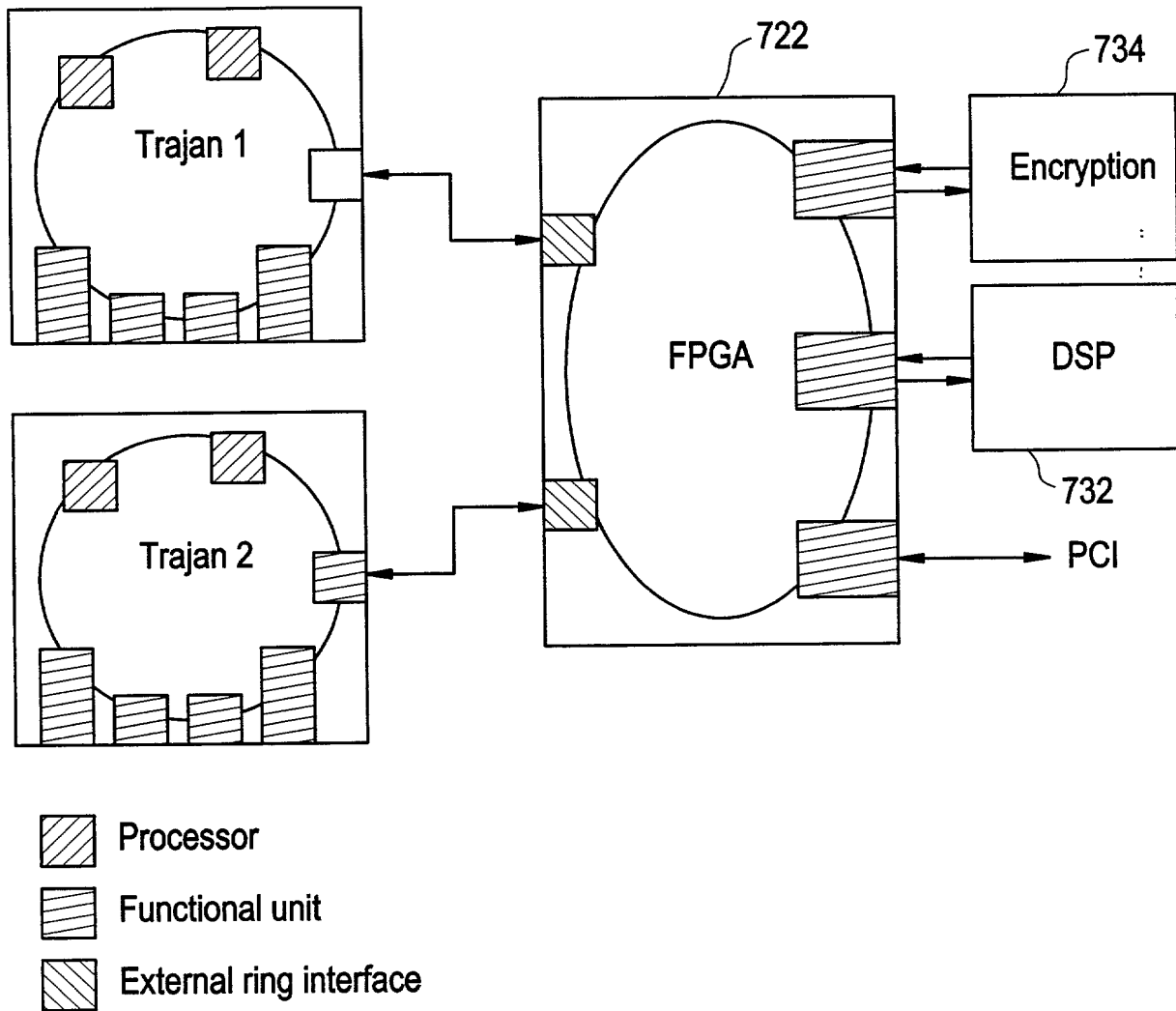


FIG. 64



40064330.092602

FIG. 65

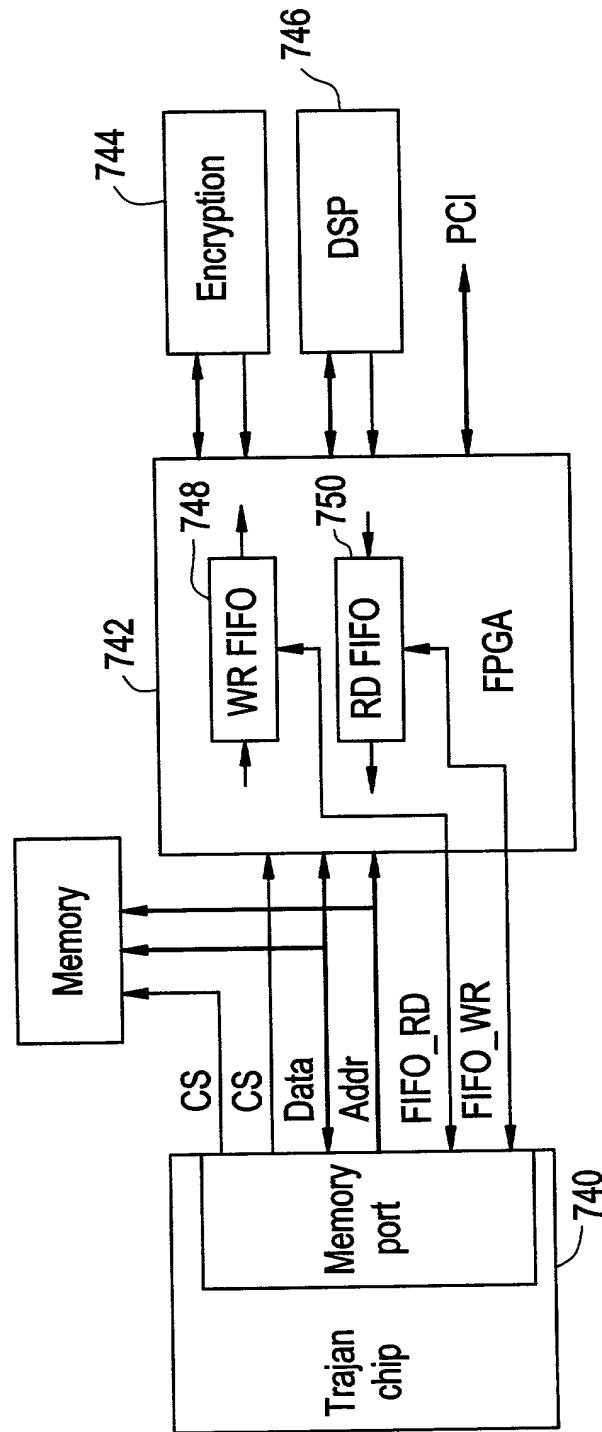


FIG. 66

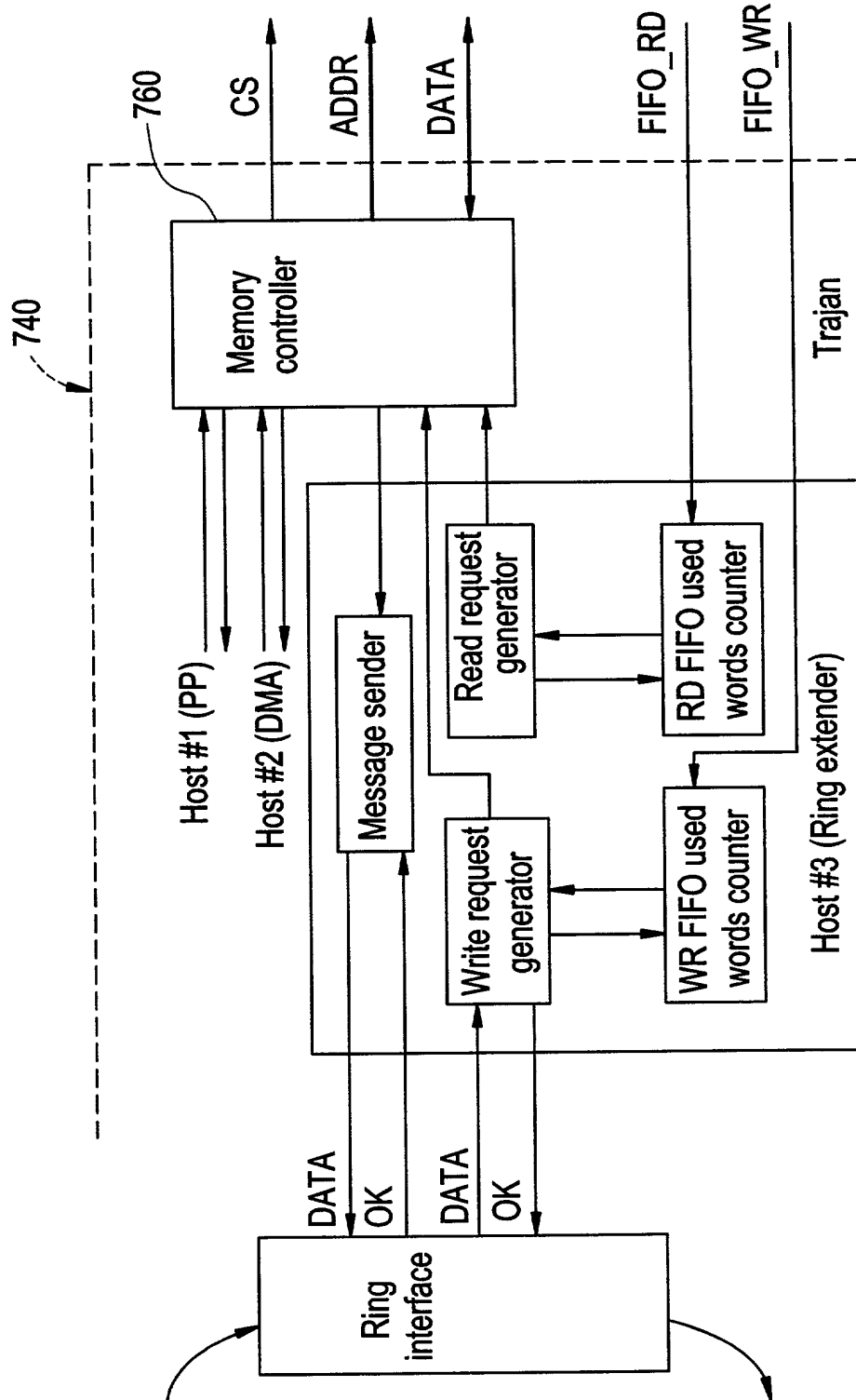


FIG. 67

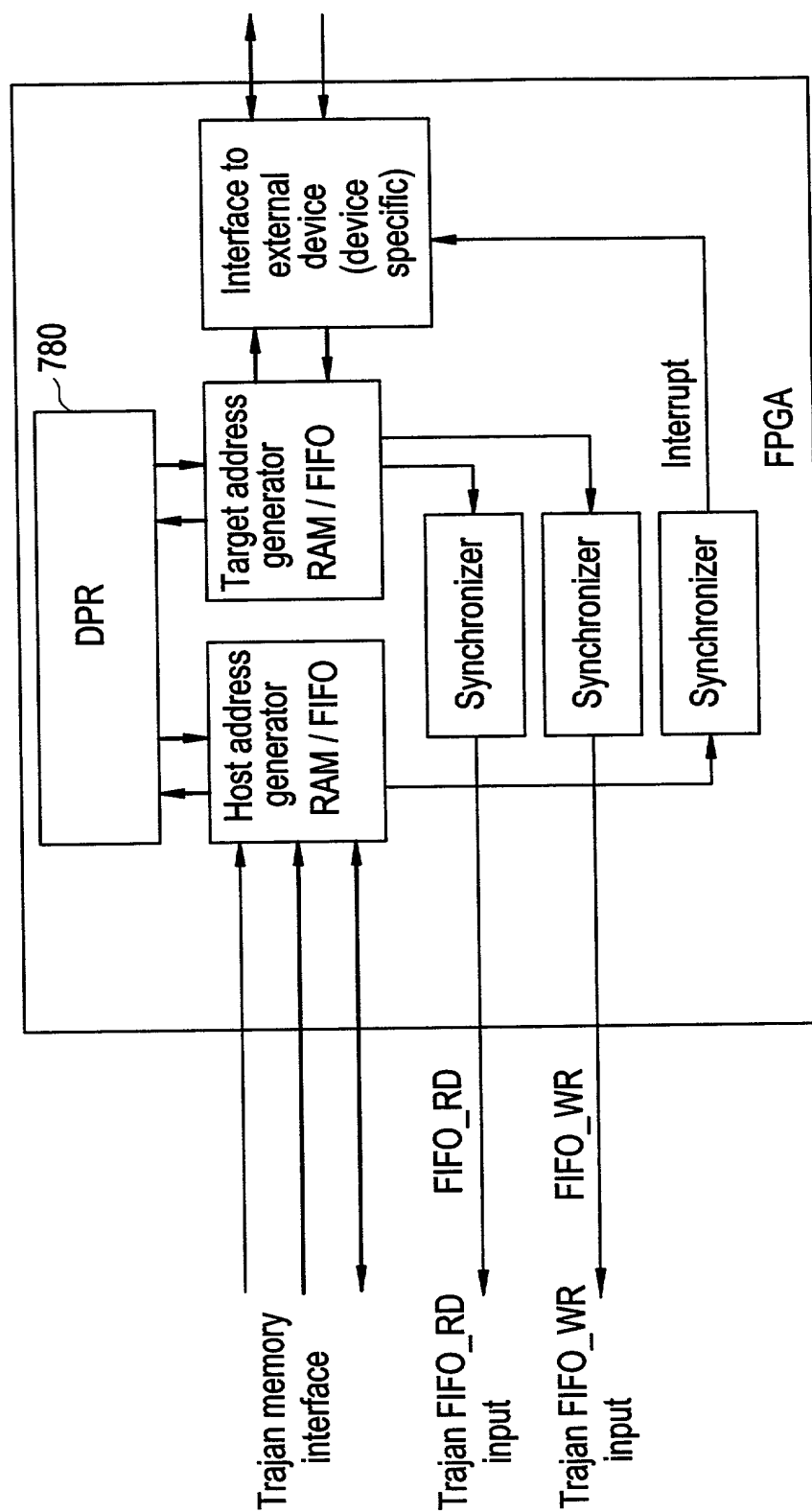
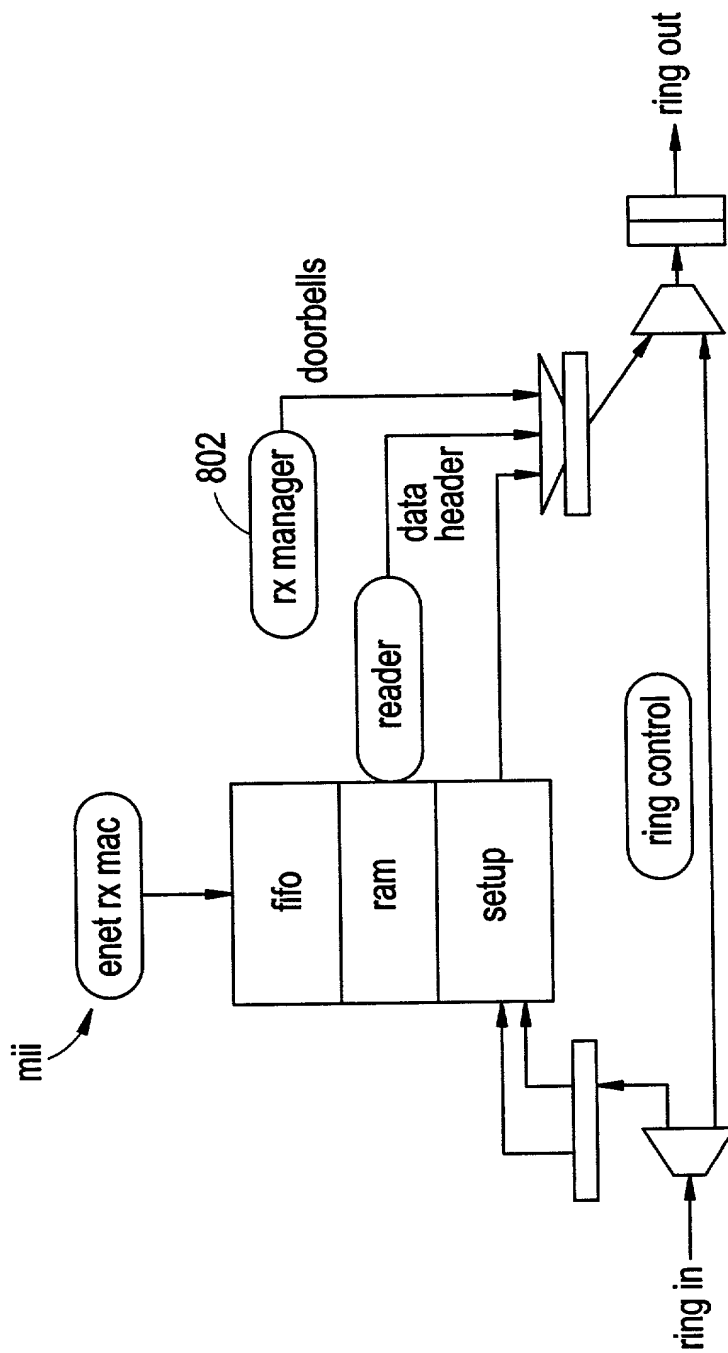


FIG. 68



20020926 064930T

FIG. 69

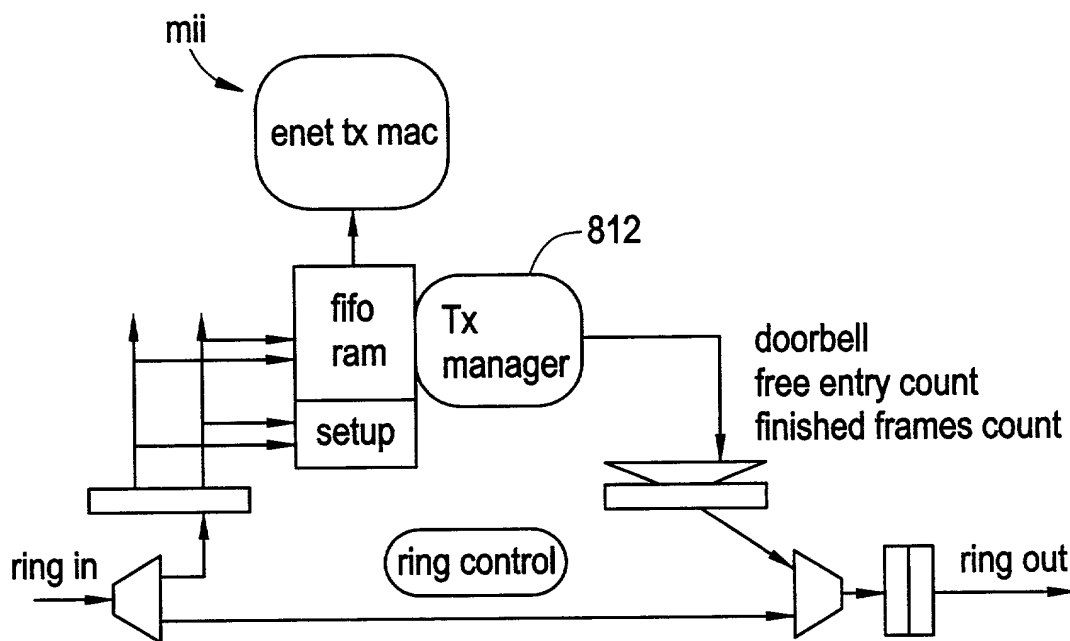
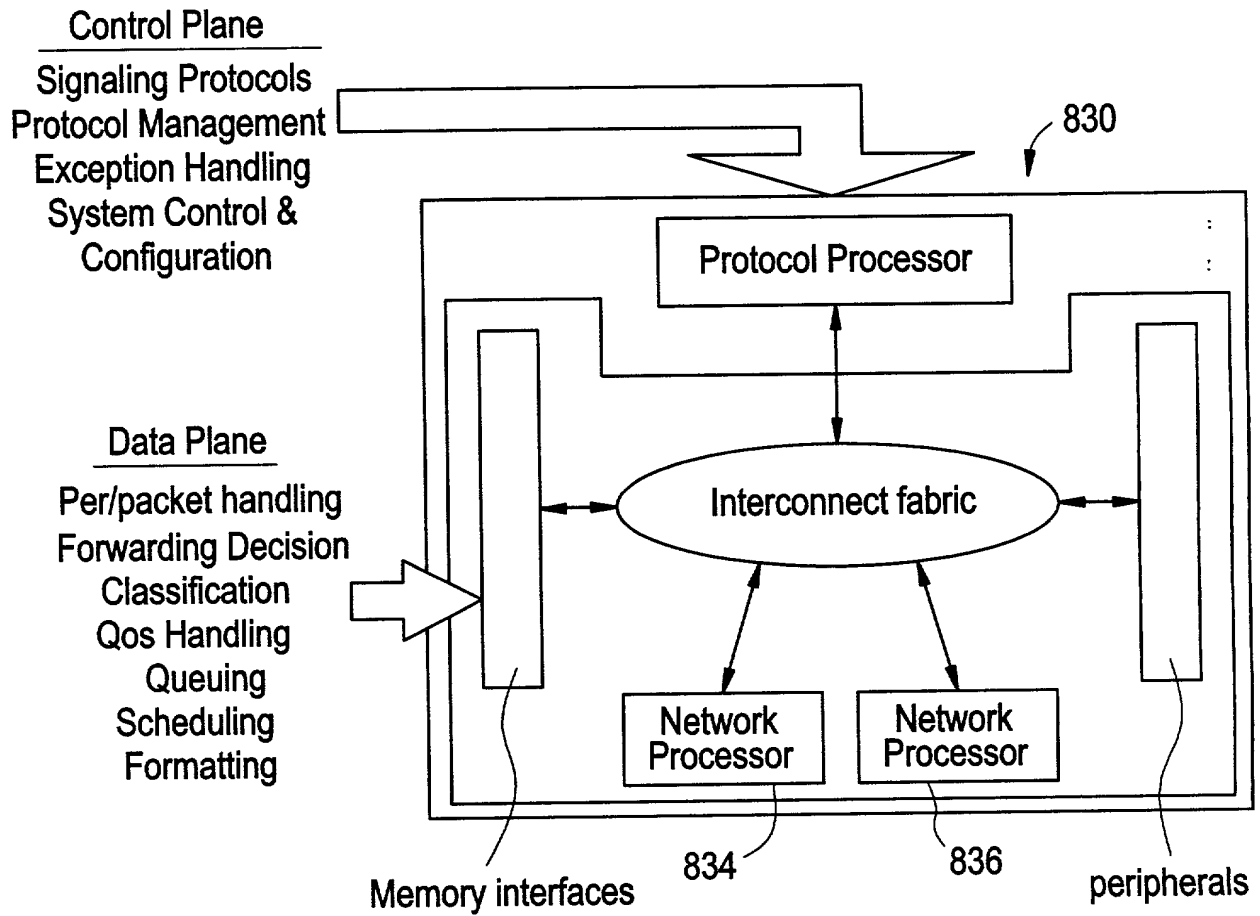


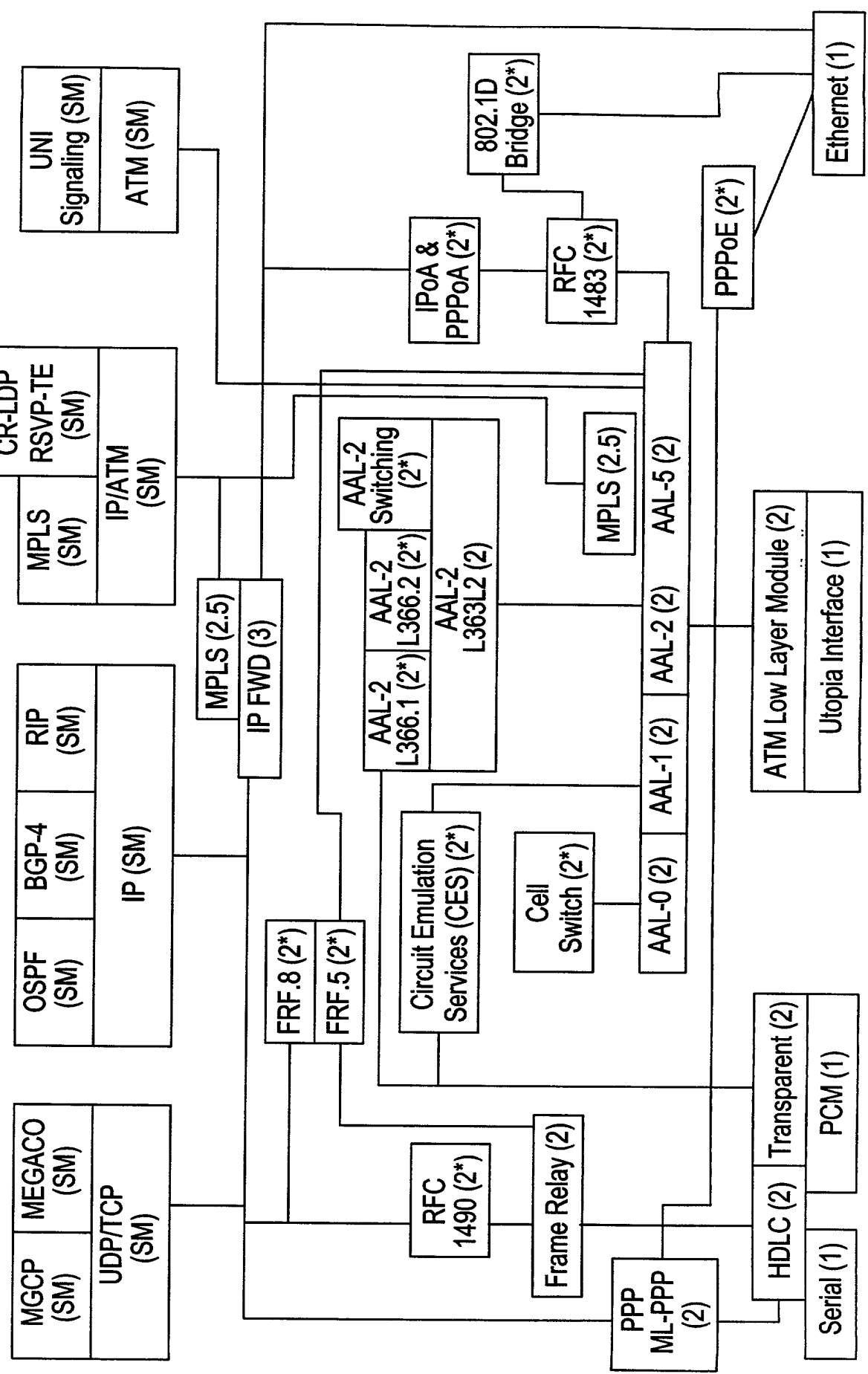
FIG. 70



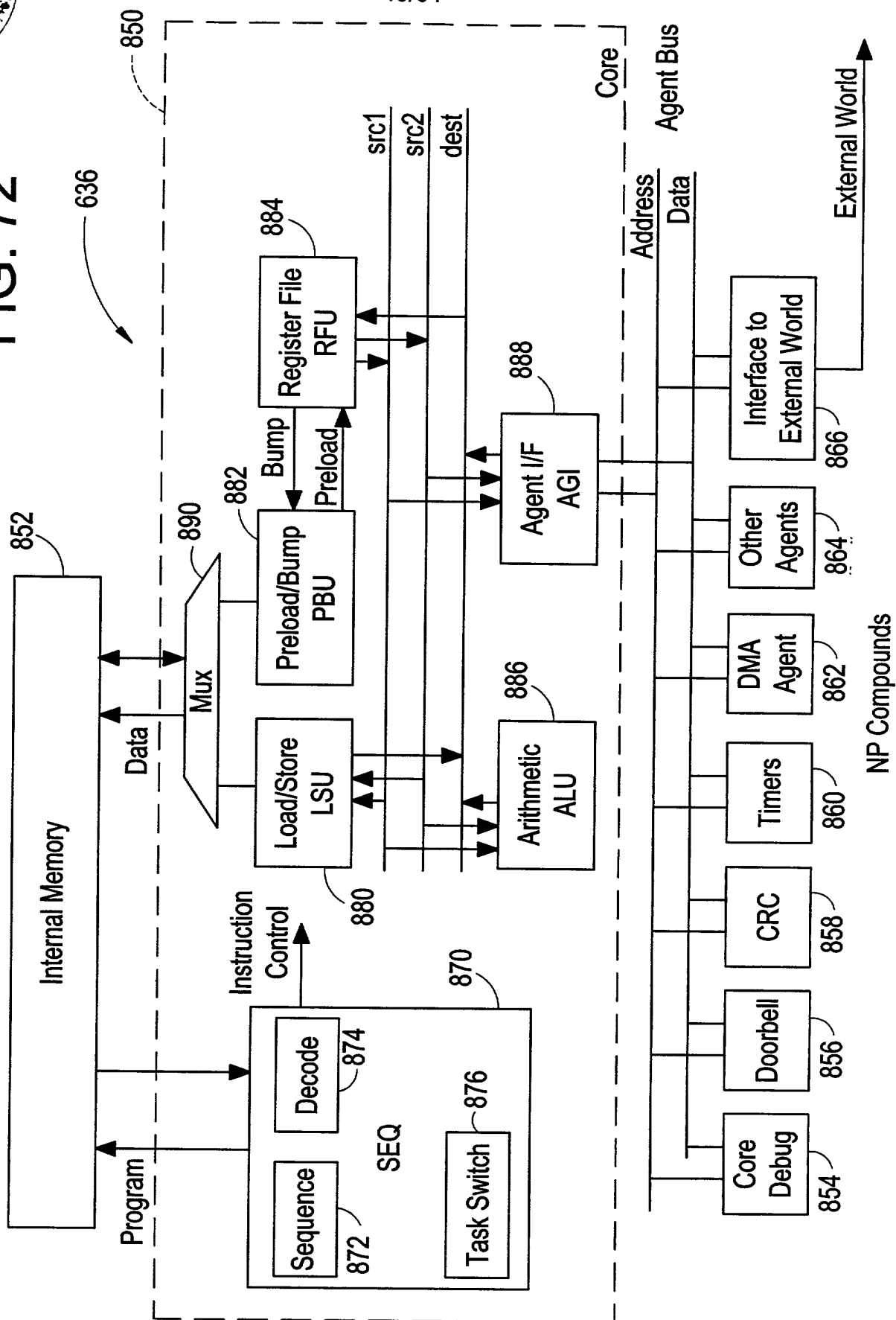
2002/06/26 14:33:37

FIG. 71

840



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Write

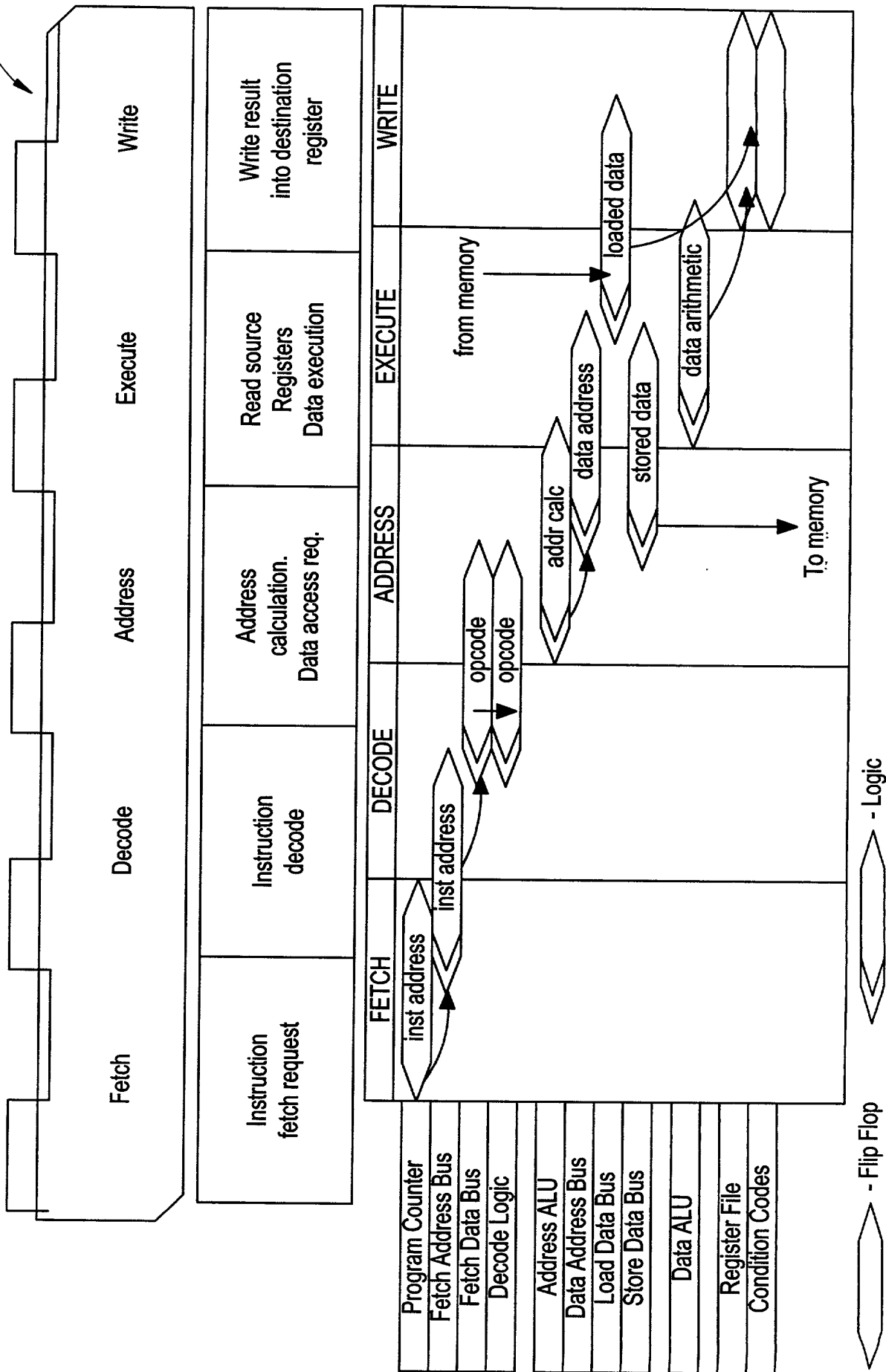


FIG. 74

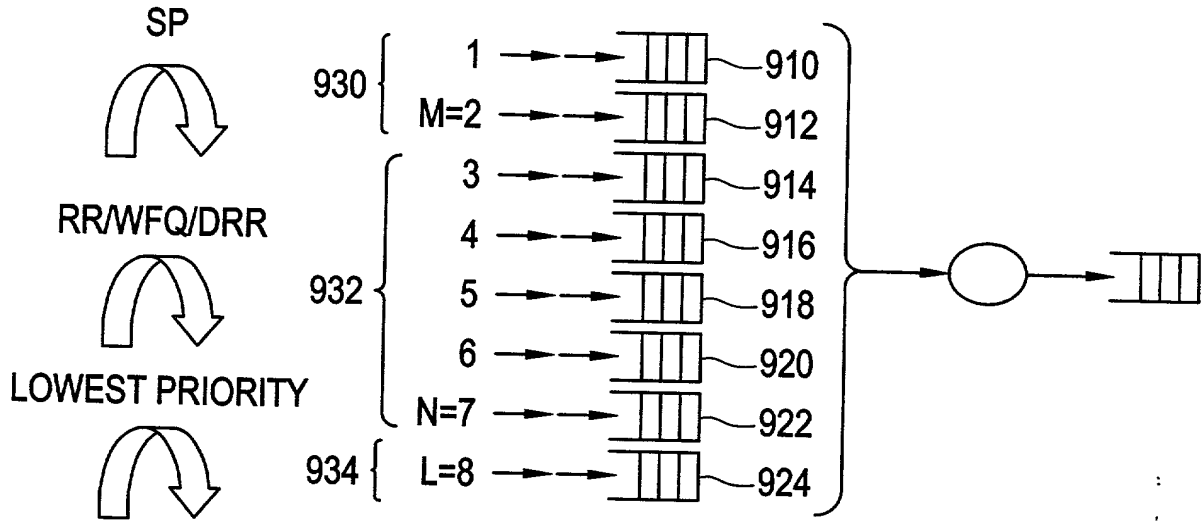
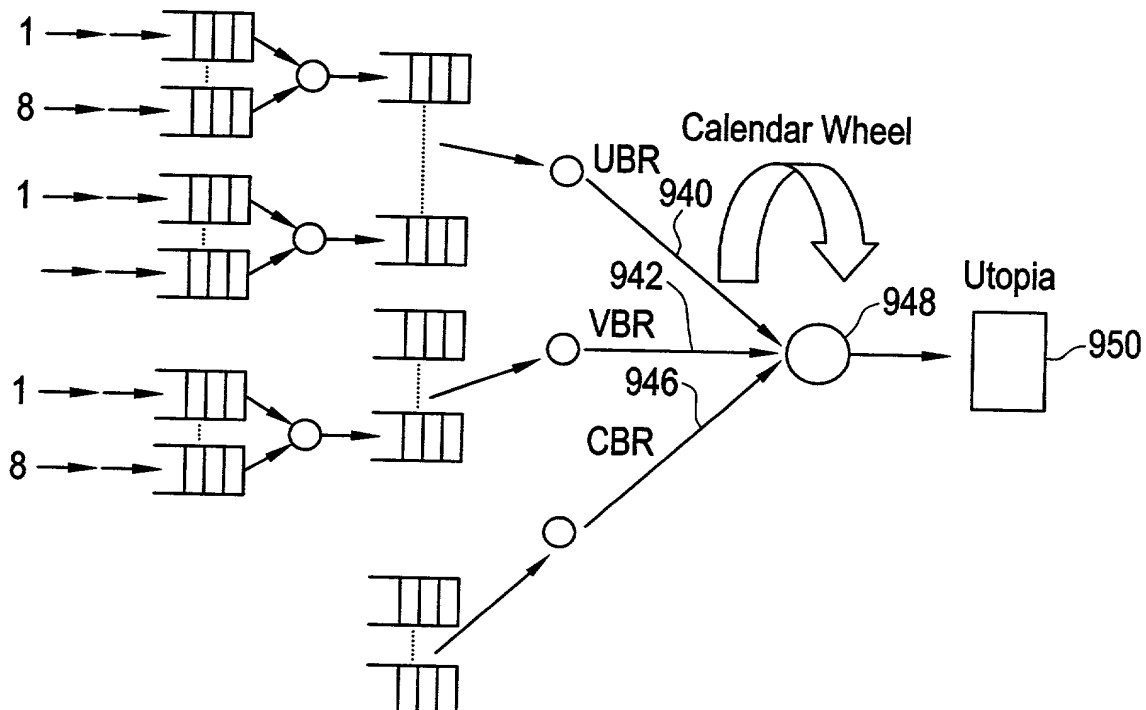


FIG. 75



200209260 "DETECTING"

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FIG. 76

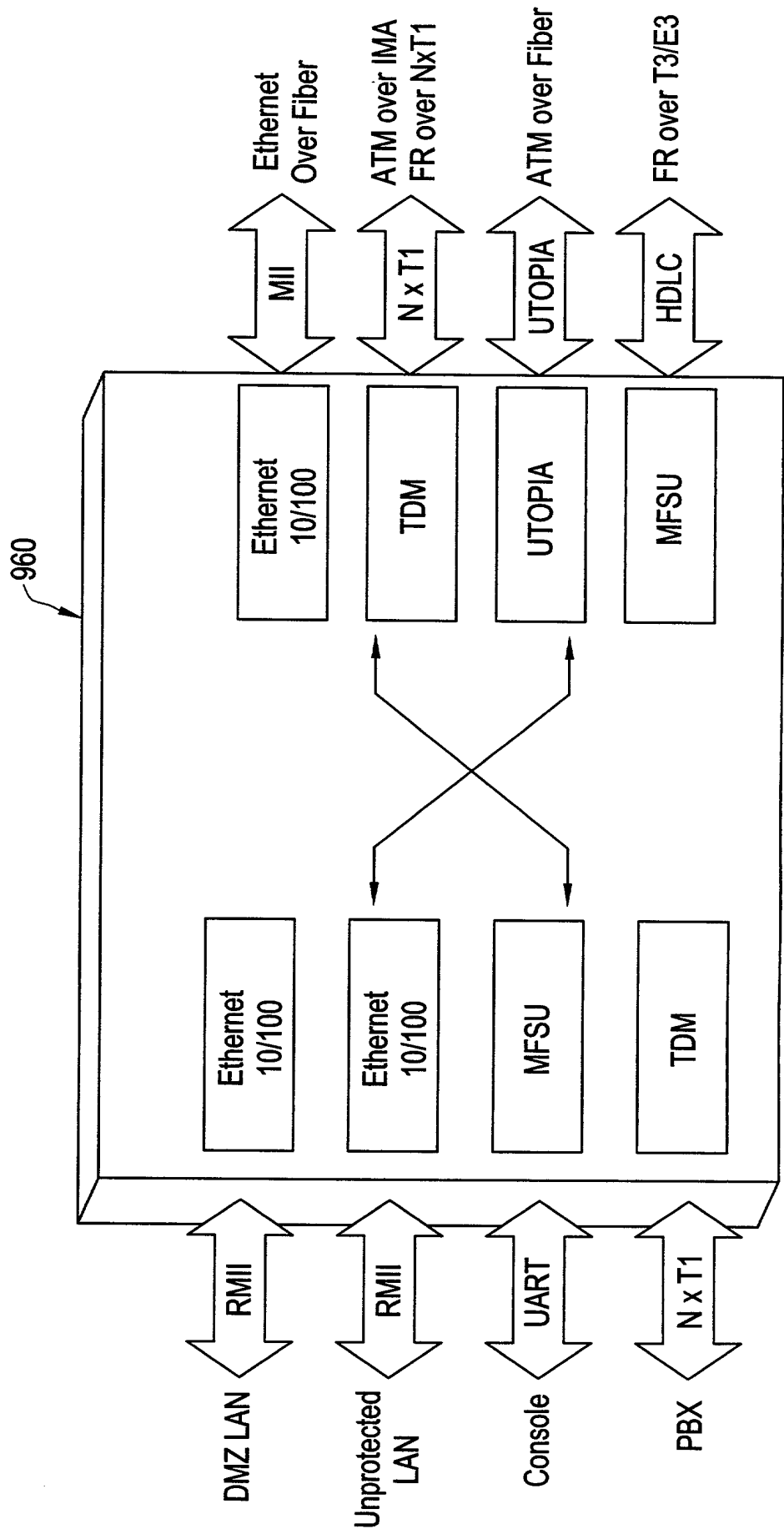


FIG. 77

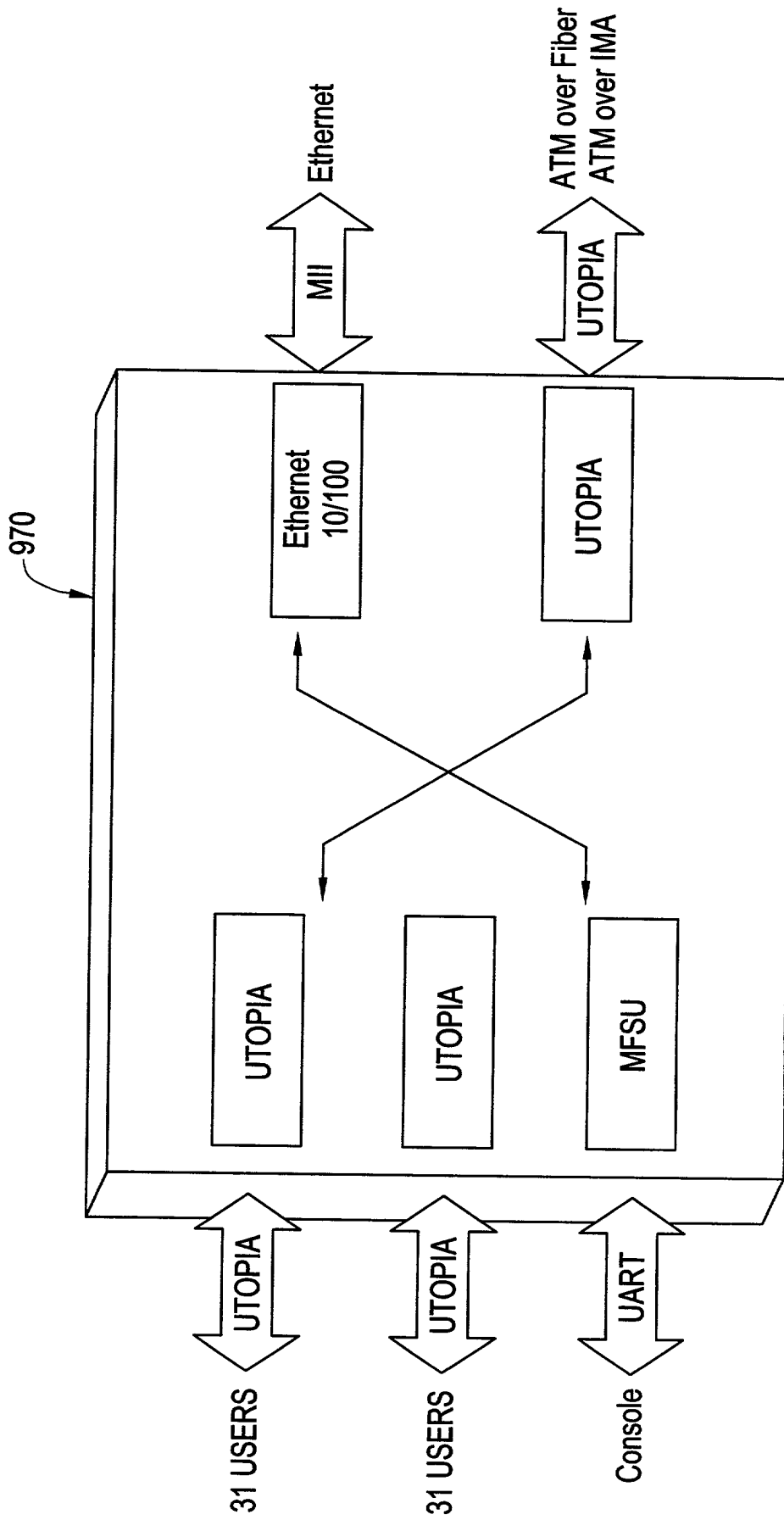


FIG. 78

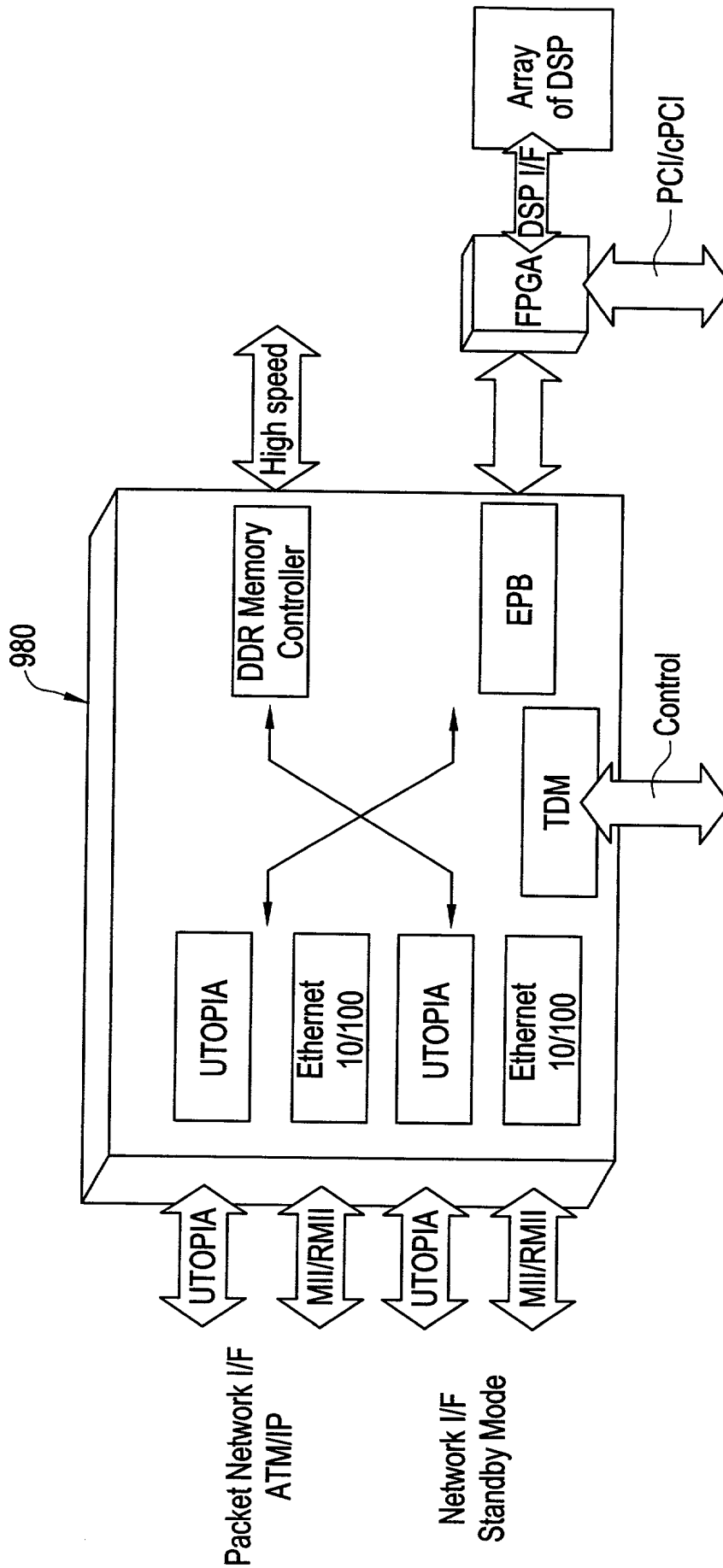


FIG. 79

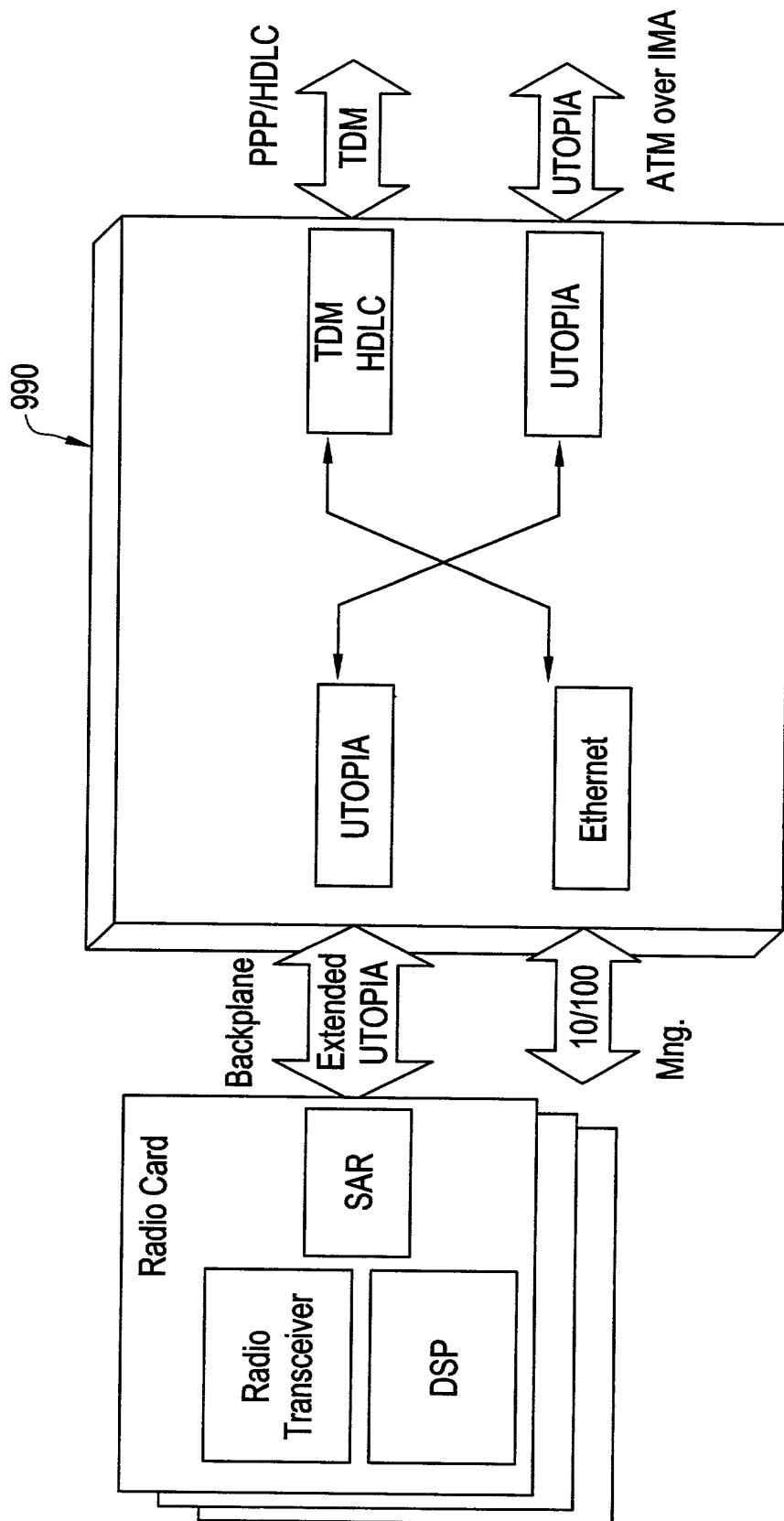


FIG. 80

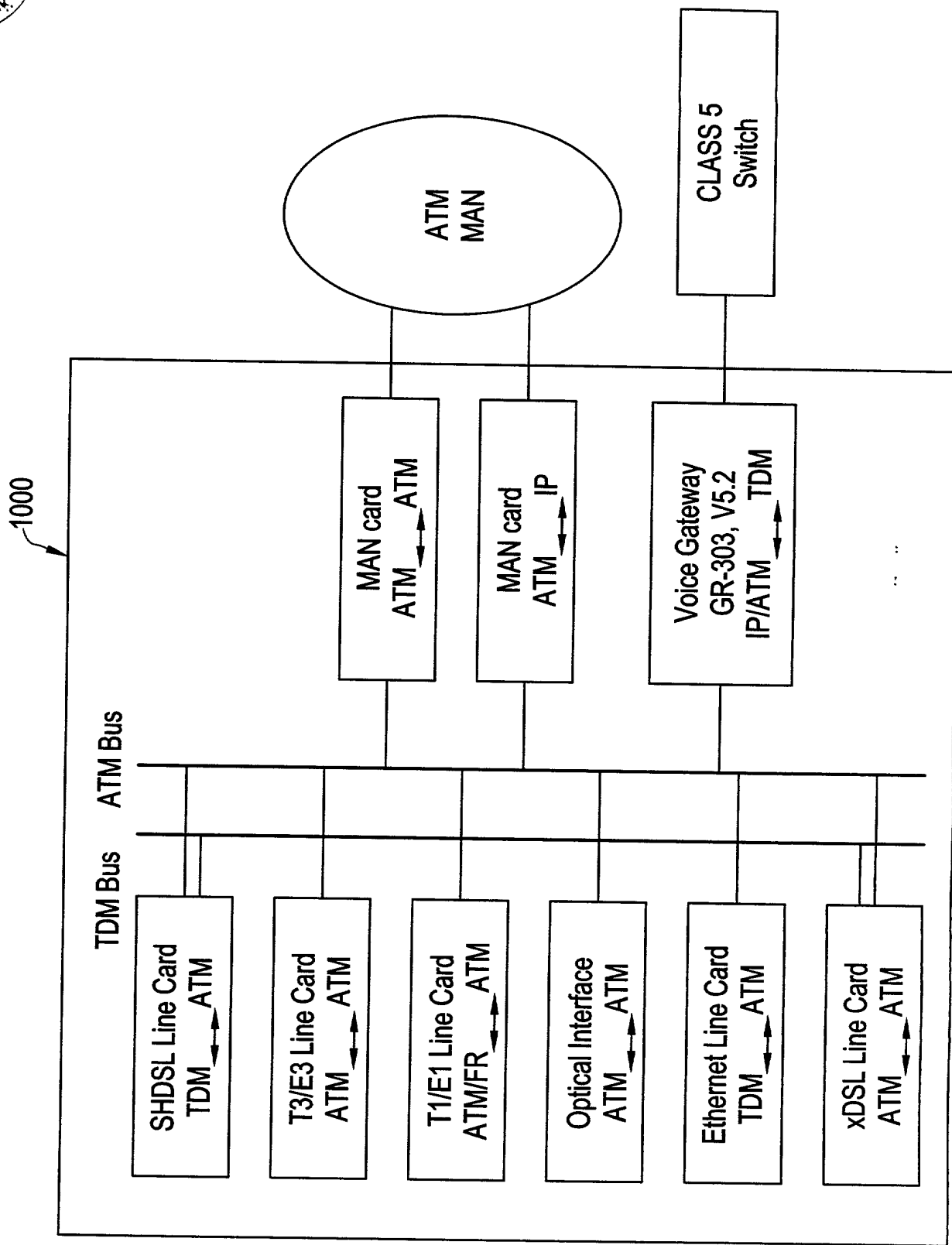


FIG. 81

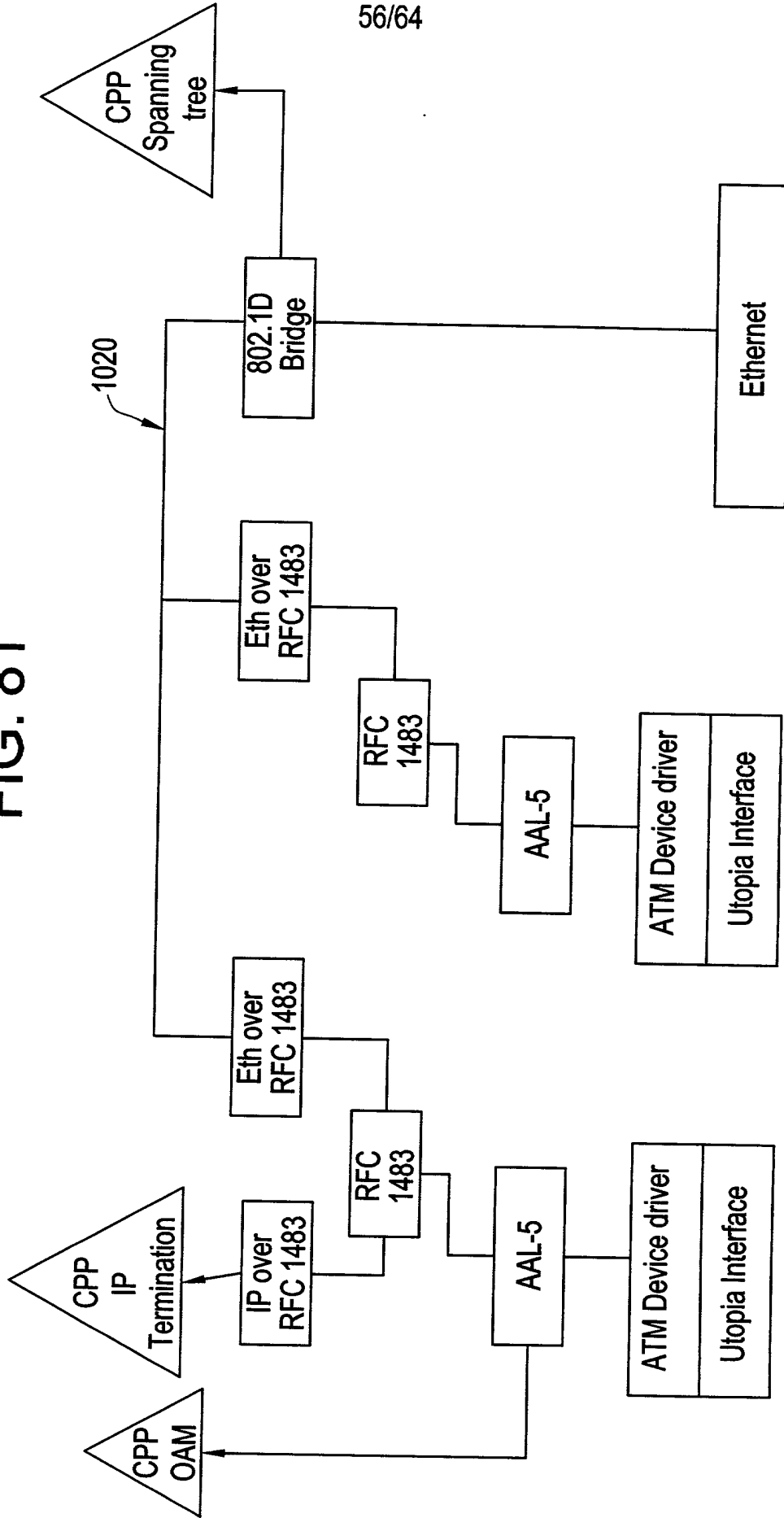


FIG. 82

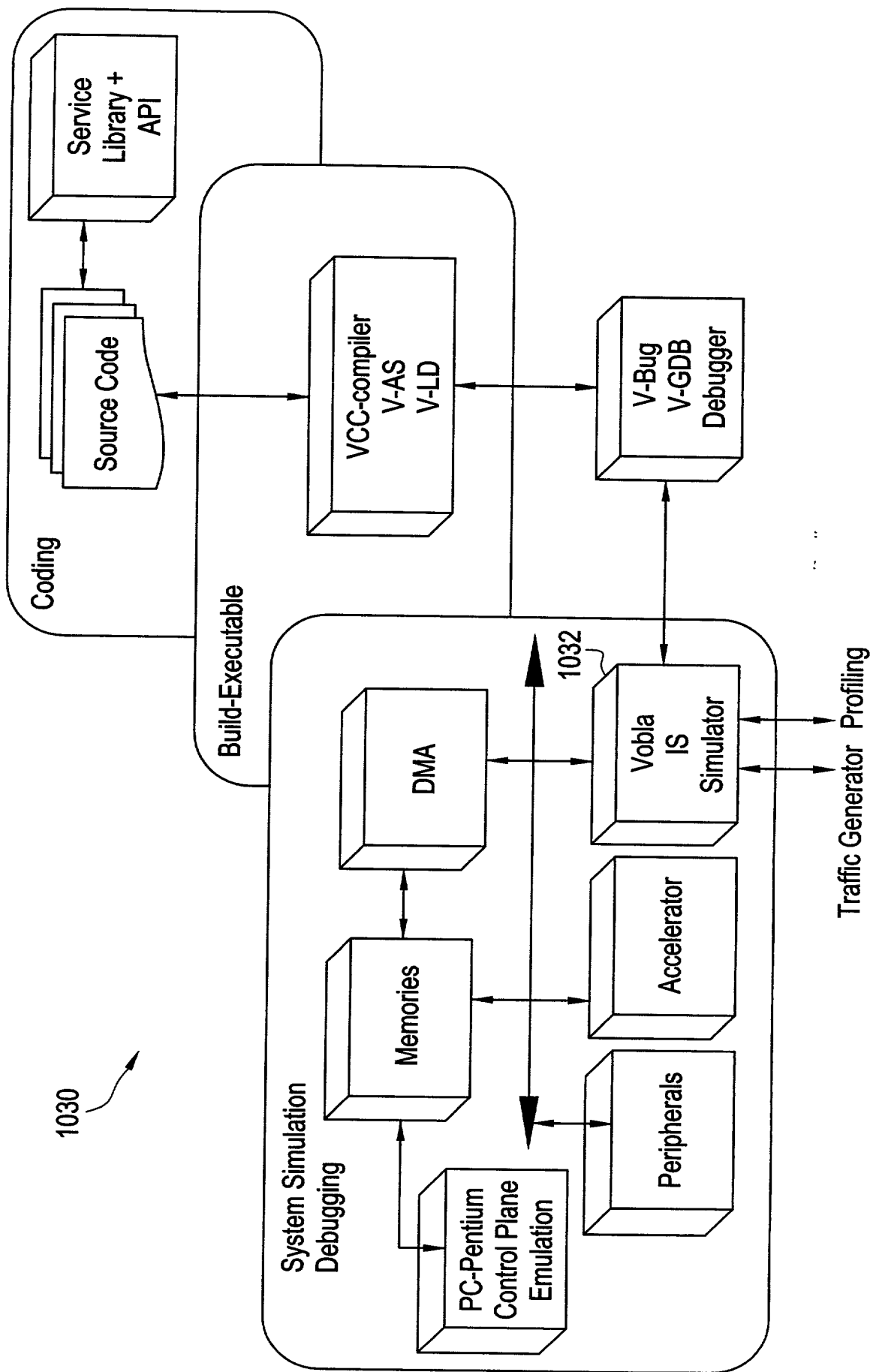


FIG. 83

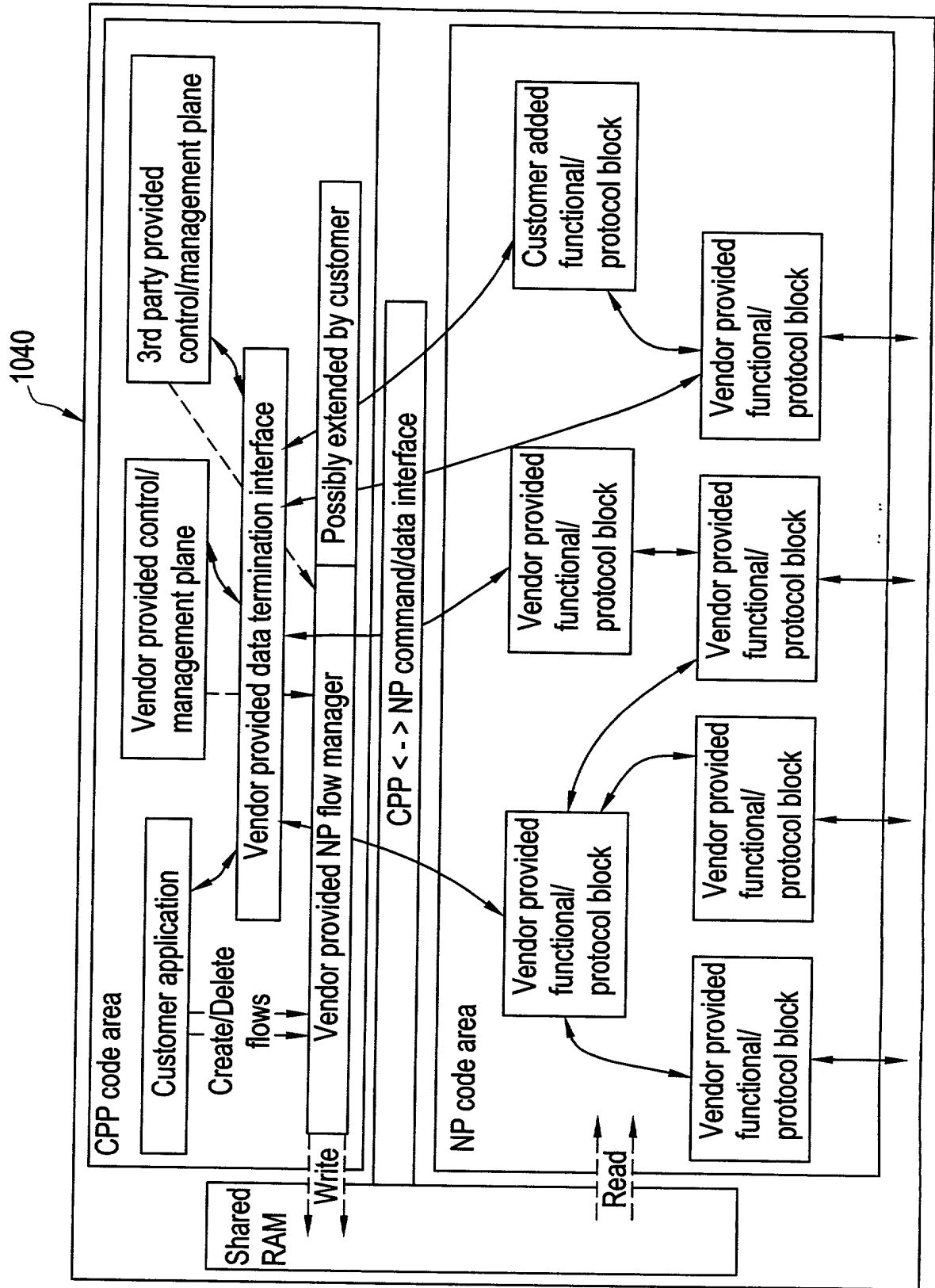


FIG. 84

1050

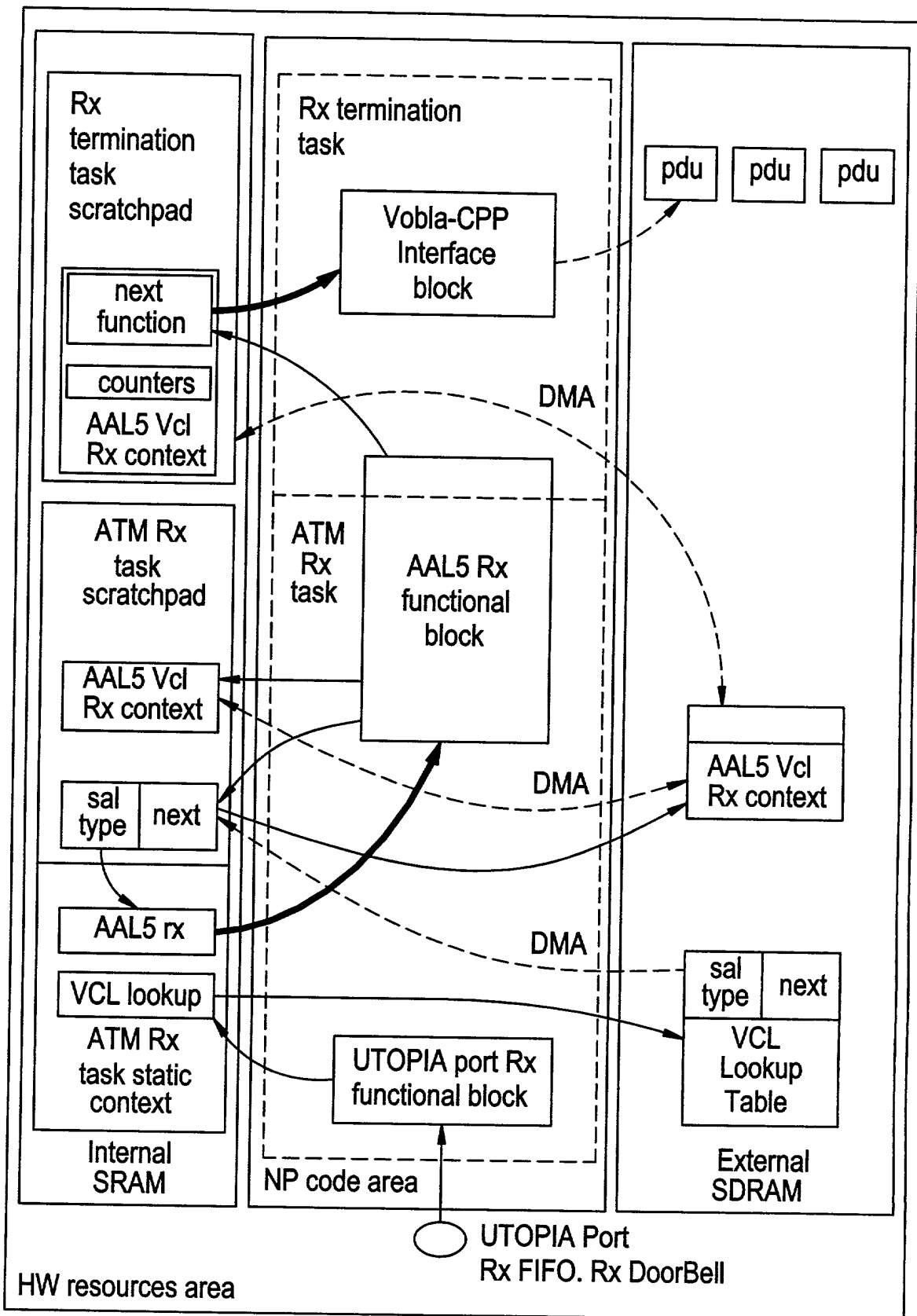


FIG. 85

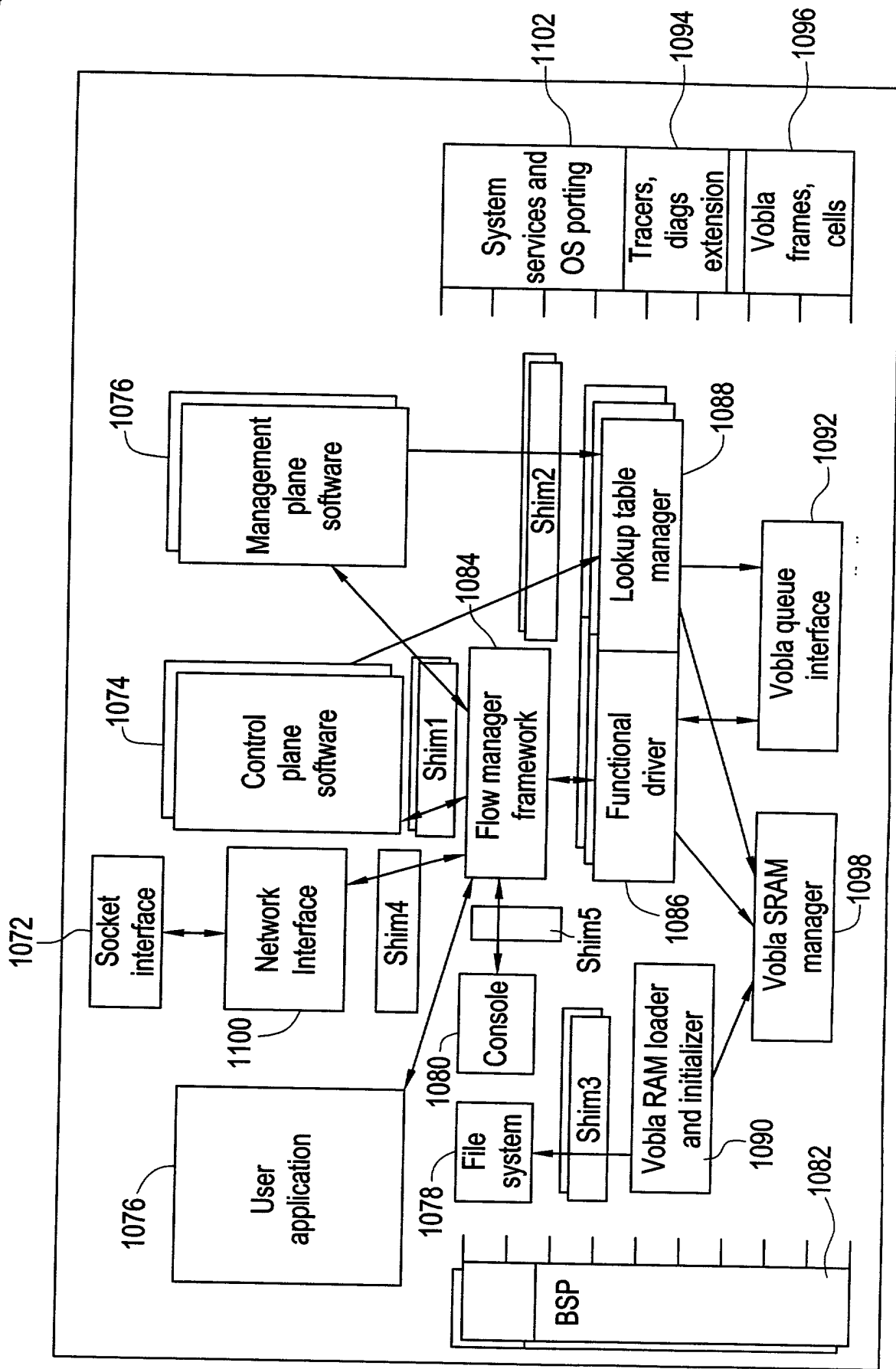
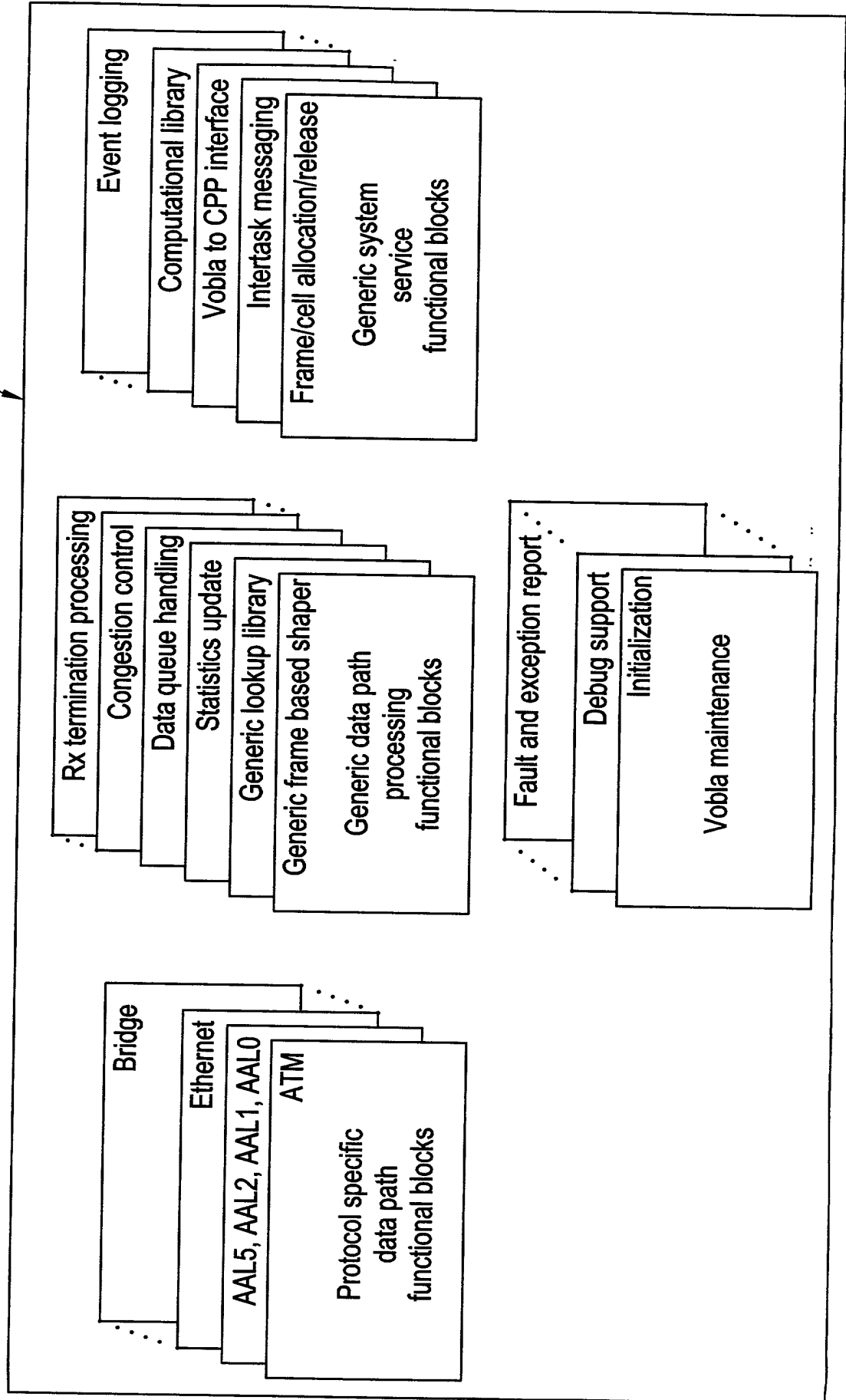


FIG. 86

1200





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FIG. 87

PRIOR ART

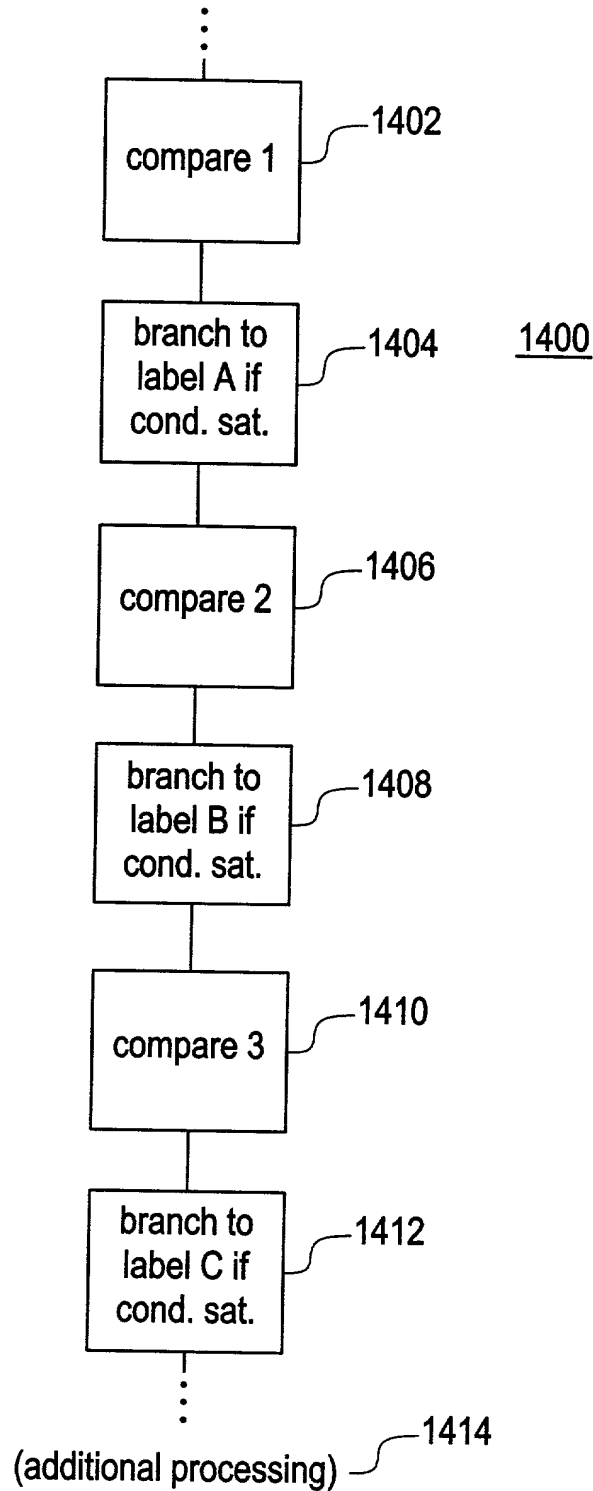


FIG. 88

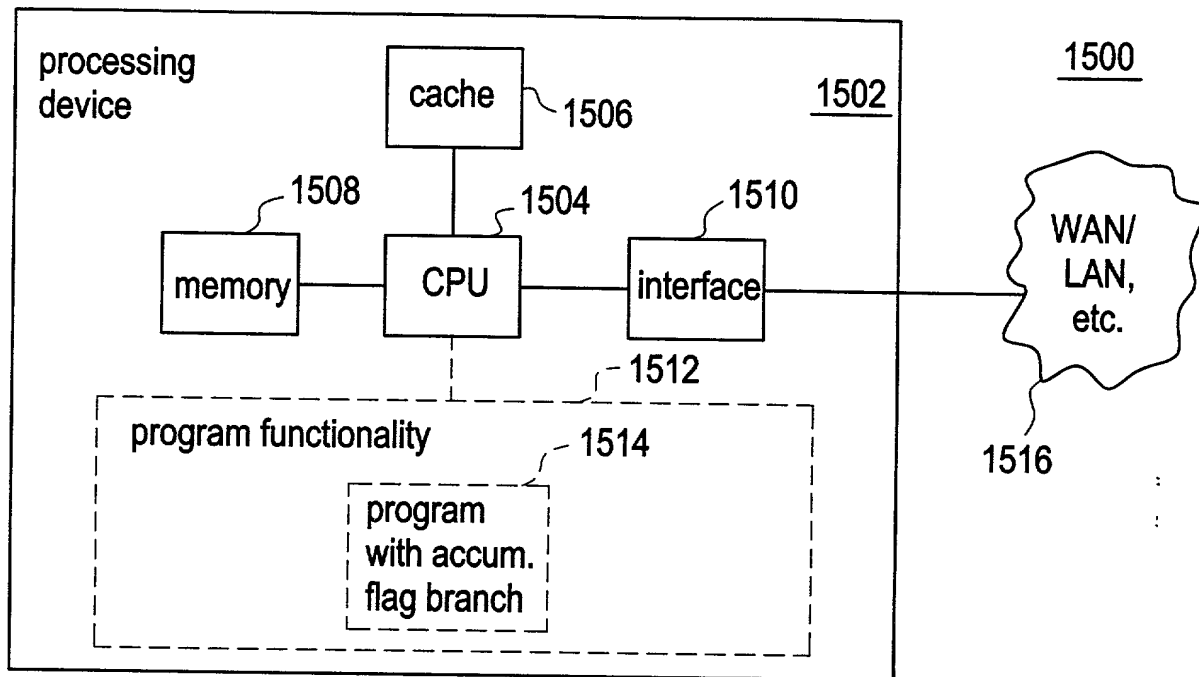


FIG. 89

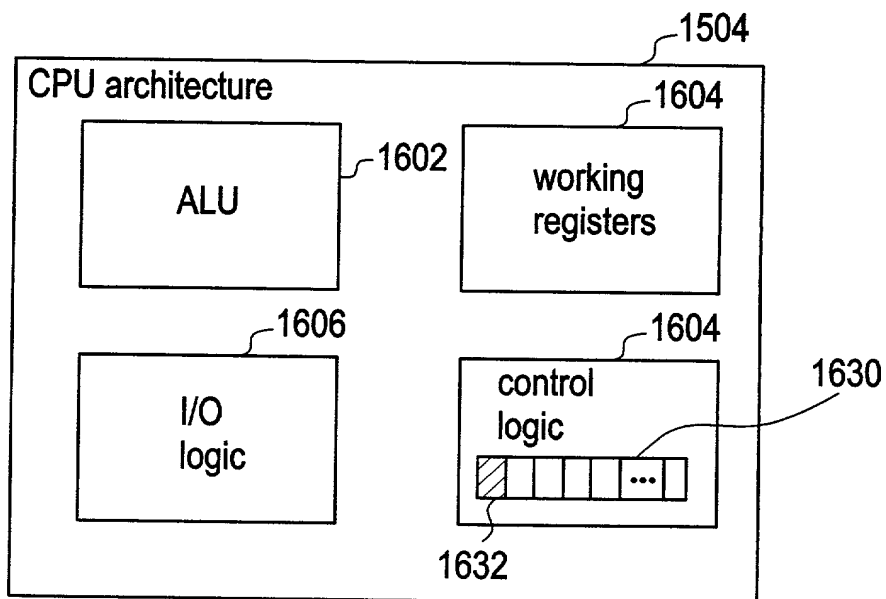




FIG. 90

